

Schematic Page List

Hide

SCHEMATIC1

01.Block Diagram

02.SKU_table

03.Change Note

04.POWER SEQUENCE

05.CPU_DDR

06.CPU_Display

07.CPU_HDA/SDIO/EMMC/LPC /S PI

08.CPU_USB3/USB2/PCIE/SATA

09.CPU_PMU/SVID/CLOCKS

10.CPU_SMBUS/I2C/CNVi

11.CPU_GPIO/JTAG

12.CPU_POWER

13.CPU_GND

14.CPU_STRAP

15.***

16.*****

17.

18.*****

19.LPDDR4_CH0_X32

20.LPDDR4_CH1_X32

Global Search

01.

02.

04.

05.

06.

07.

08.

09.

10.

11.

12.

Toggle FullScreen

Pre Page

Next Page

MoveTo

BLOCK DIAGRAM

X540MB

CPU

GEMINI LAKE

LPDDR4 on board

LPDDR4 on board

HDD

ODD

WLAN, BT

CardReader

USB 3.0 Port

USB2.0 Port

USB2.0 Port

IO Board

Camera

EDP Panel

HDMI

Combo Jack

INT.SPEAKER

Debug Conn.

SPI ROM

Keyboard

SPI ROM

Touchpad

ALC3251

ENE_KB902AQ C

EDP

DDIO

HDA

LPC

SPI

SPI

I2C

ASUS

Product Name

Rev

1.0

Title : Block Diagram

Size

Dept.: Hardware

Engineer: Arian_Chiang

Date: Friday, February 23, 2018

Sheet 1 of 63

Schematic Page List

Hide

Global Search

01.

02.

04.

05.

06.

07.

08.

09.

10.

11.

12.

Toggle FullScreen

Pre Page

Next Page

MoveTo

SCHEMATIC1

01.Block Diagram

02.SKU_table

03.Change Note

04.POWER SEQUENCE

05.CPU_DDR

06.CPU_Display

07.CPU_HDA/SDIO/EMMC/LPC /S
PI

08.CPU_USB3/USB2/PCIE/SATA

09.CPU_PMU/SVID/CLOCKS

10.CPU_SMBUS/I2C/CNVi

11.CPU_GPIO/JTAG

12.CPU_POWER

13.CPU_GND

14.CPU_STRAP

15.***

16.*****

17.

18.*****

19.LPDDR4_CH0_X32

201 PNDRA CH1 Y32

EE PART

X540MB SKU Table

[illegible]

Thermal sensor		
----------------	--	--

Hide

Global Search

01.

02.

04.

05.

06.

07.

08.

09.

10.

11.

12.

Toggle FullScreen

Pre Page

Next Page

MoveTo

01.Block Diagram

02.SKU_table

03.Change Note

04.POWER SEQUENCE

05.CPU DDR

06.CPU_Display

07.CPU_HDA/SDIO/EMMC/LPC /S
PI

08.CPU USB3/USB2/PCIE/SATA

09.CPU_PMU/SVID/CLOCKS

10.CPU SMBUS/I2C/CNVi

11.CPU GPIO/JTAG

12.CPU_POWER

13.CPU_GND

14.CPU STRAP

15.***

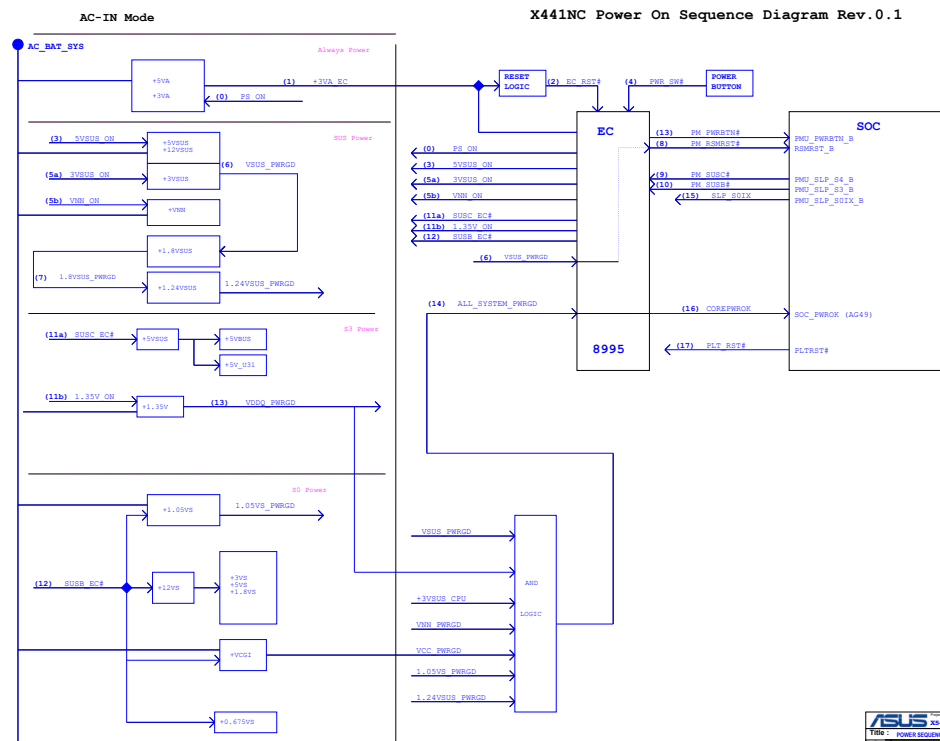
16.*****

17.

18.*****

19.LPDDR4 CH0 X32

201 PONDRA CH1 Y32



Schematic Page List

Hide

SCHEMATIC1

- 01.Block Diagram
- 02.SKU_table
- 03.Change Note
- 04.POWER SEQUENCE
- 05.CPU_DDR
- 06.CPU_Display
- 07.CPU_HDA/SDIO/EMMC/LPC /S
PI
- 08.CPU_USB3/USB2/PCIE/SATA
- 09.CPU_PMU/SVID/CLOCKS
- 10.CPU_SMBUS/I2C/CNVi
- 11.CPU_GPIO/JTAG
- 12.CPU_POWER
- 13.CPU_GND
- 14.CPU_STRAP
- 15.***
- 16.*****
- 17.
- 18.*****
- 19.LPDDR4_CH0_X32
- 20.LPDDR4_CH1_X32

Global Search

01.

02.

04.

05.

06.

07.

08.

09.

10.

11.

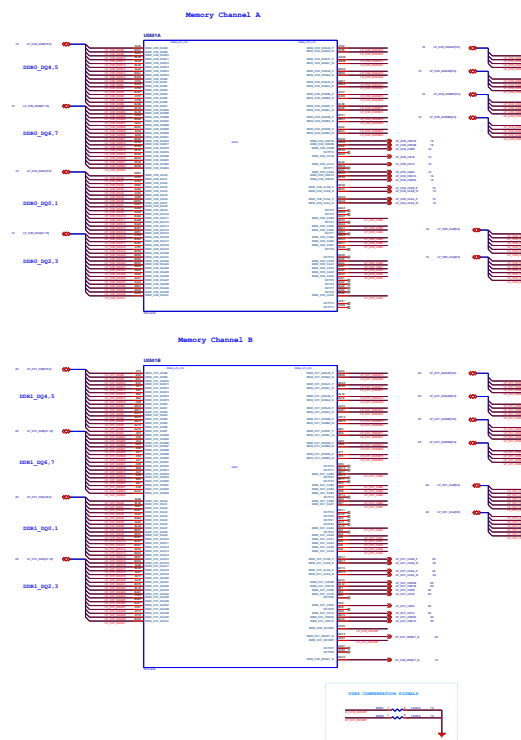
12.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

Global Search

01.

02.

04.

05.

06.

07.

08.

09.

10.

11.

12.

Toggle FullScreen

Pre Page

Next Page

MoveTo

SCHEMATIC1

01.Block Diagram

02.SKU_table

03.Change Note

04.POWER SEQUENCE

05.CPU_DDR

06.CPU_Display

07.CPU_HDA/SDIO/EMMC/LPC /S
PI

08.CPU_USB3/USB2/PCIE/SATA

09.CPU_PMU/SVID/CLOCKS

10.CPU_SMBUS/I2C/CNVi

11.CPU_GPIO/JTAG

12.CPU_POWER

13.CPU_GND

14.CPU_STRAP

15.***

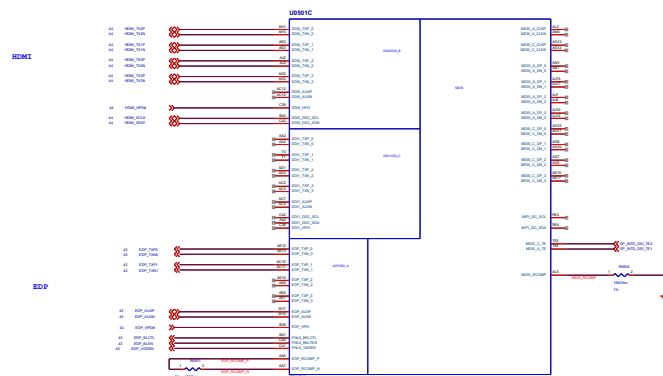
16.*****

17.

18.*****

19.LPDDR4_CH0_X32

201 PDDR4 CH1 X32



Schematic Page List

Hide

Global Search

01.

02.

04.

05.

06.

07.

08.

09.

10.

11.

12.

Toggle FullScreen

Pre Page

Next Page

MoveTo

SCHEMATIC1

01.Block Diagram

02.SKU_table

03.Change Note

04.POWER SEQUENCE

05.CPU_DDR

06.CPU_Display

07.CPU_HDA/SDIO/EMMC/LPC /S
PI

08.CPU_USB3/USB2/PCIE/SATA

09.CPU_PMU/SVID/CLOCKS

10.CPU_SMBUS/I2C/CNVi

11.CPU_GPIO/JTAG

12.CPU_POWER

13.CPU_GND

14.CPU_STRAP

15.***

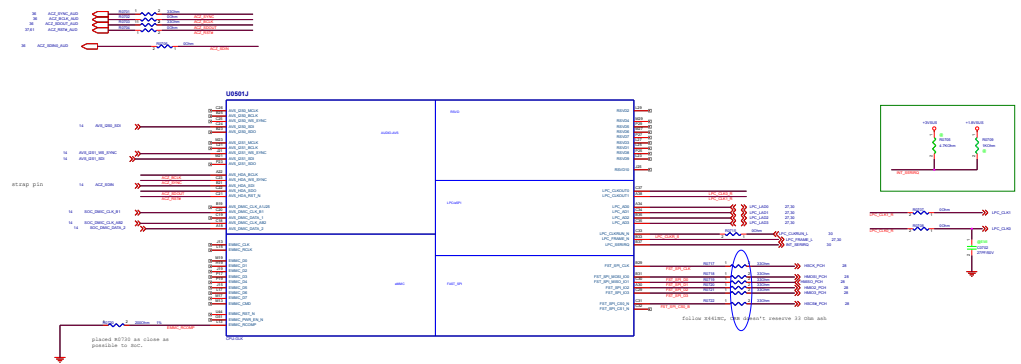
16.*****

17.

18.*****

19.LPDDR4 CH0 X32

201 PDDR4 CH1 X32



Schematic Page List

Hide

SCHEMATIC1

- 01.Block Diagram
- 02.SKU_table
- 03.Change Note
- 04.POWER SEQUENCE
- 05.CPU_DDR
- 06.CPU_Display
- 07.CPU_HDA/SDIO/EMMC/LPC /S PI
- 08.CPU_USB3/USB2/PCIE/SATA
- 09.CPU_PMU/SVID/CLOCKS
- 10.CPU_SMBUS/I2C/CNVi
- 11.CPU_GPIO/JTAG
- 12.CPU_POWER
- 13.CPU_GND
- 14.CPU_STRAP
- 15.***
- 16.*****
- 17.
- 18.*****
- 19.LPDDR4_CH0_X32
- 20.LPDDR4_CH1_X32

Global Search

01.

02.

04.

05.

06.

07.

08.

09.

10.

11.

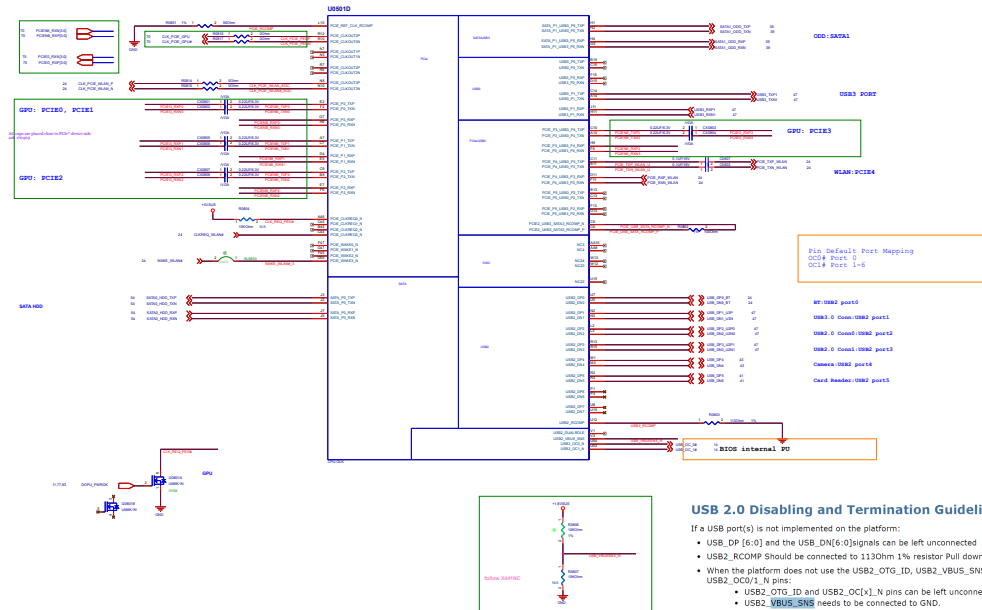
12.

Toggle FullScreen

Pre Page

Next Page

MoveTo



USB 2.0 Disabling and Termination Guidelines

If a USB port(s) is not implemented on the platform:

- USB_DP [6:0] and the USB_DN[6:0] signals can be left unconnected
- USB2_RCOMP should be connected to 1130hm 1% resistor Pull down to ground
- When the platform does not use the USB2_OTG_ID, USB2_VBUS_SNS, and USB2_OCO/1_N pins:
 - USB2_OTG_ID and USB2_OCO[1:N] pins can be left unconnected.
 - USB2_VBUS_SNS needs to be connected to GND.
- The USB2_OTG_ID pin has an internal 100kohm pull up and the USB2_OCO[0:1] N pins have an internal 20k pull up, so an external pull up is not required. However, if customers are concerned on platform EMI, it is recommended to use external 10k pull up resistor to V1P8A

Schematic Page List

Hide

Global Search

01.

02.

04.

05.

SCHEMATIC1

01.Block Diagram

02.SKU table

03.Change Note

04.POWER SEQUENCE

05.CPU DDR

06.CPU_Display

07.CPU_HDA/SDIO/EMMC/LPC /S
PI

08.CPU USB3/USB2/PCIE/SATA

09.CPU PMU/SVID/CLOCKS

10.CPU SMBUS/I2C/CNVi

11.CPU GPIO/JTAG

12.CPU POWER

13.CPU_GND

14.CPU_STRAP

15.***

16.*****

17.

18.*****

19.LPDDR4 CH0 X32

201 PONDRA CH1 Y32

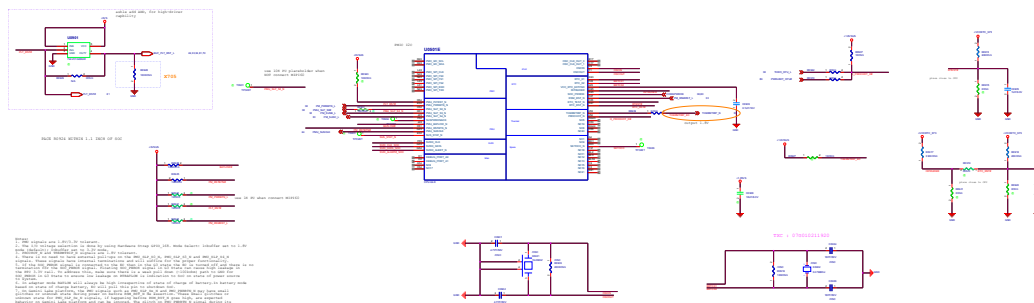
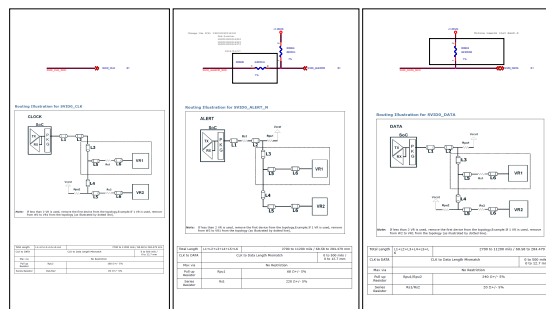


Table 2-22. Gemini Lake RTC Interface

[illegible]

Schematic Page List

Hide

Global Search

01.

02.

04.

05.

06.

07.

08.

09.

10.

11.

12.

SCHEMATIC1

01.Block Diagram

02.SKU_table

03.Change Note

04.POWER SEQUENCE

05.CPU_DDR

06.CPU_Display

07.CPU_HDA/SDIO/EMMC/LPC /S
PI

08.CPU_USB3/USB2/PCIE/SATA

09.CPU_PMU/SVID/CLOCKS

10.CPU_SMBUS/I2C/CNVi

11.CPU_GPIO/JTAG

12.CPU_POWER

13.CPU_GND

14.CPU_STRAP

15.***

16.*****

17.

18.*****

19.LPDDR4_CH0_X32

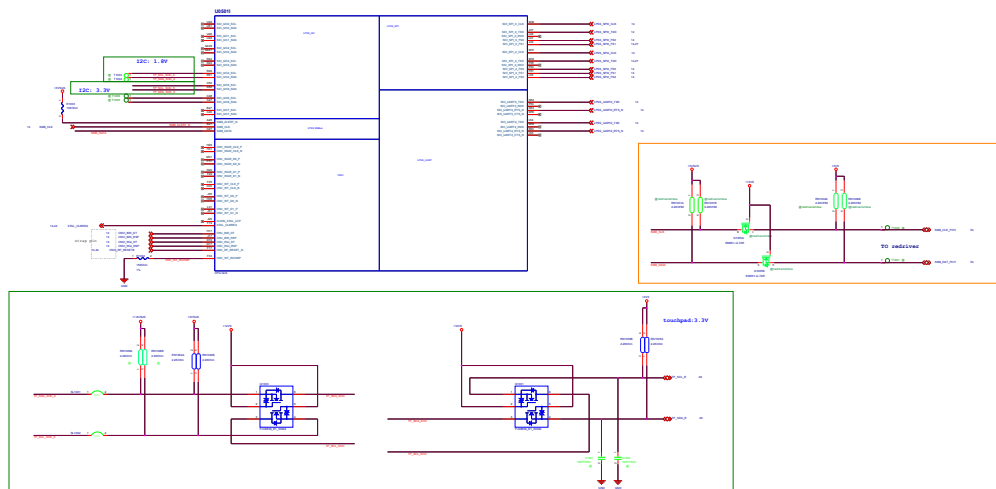
201 PONDRA CH1 Y32

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

SCHEMATIC1

- 01.Block Diagram
- 02.SKU_table
- 03.Change Note
- 04.POWER SEQUENCE
- 05.CPU_DDR
- 06.CPU_Display
- 07.CPU_HDA/SDIO/EMMC/LPC /S
PI
- 08.CPU_USB3/USB2/PCIE/SATA
- 09.CPU_PMU/SVID/CLOCKS
- 10.CPU_SMBUS/I2C/CNVi
- 11.CPU_GPIO/JTAG
- 12.CPU_POWER
- 13.CPU_GND
- 14.CPU_STRAP
- 15.***
- 16.*****
- 17.
- 18.*****
- 19.LPDDR4_CH0_X32
- 20.LPDDR4_CH1_X32

Global Search

01.

02.

04.

05.

06.

07.

08.

09.

10.

11.

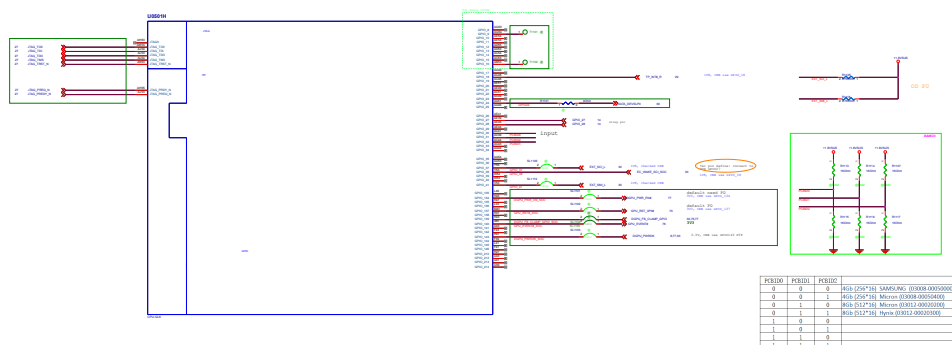
12.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

SCHEMATIC1

- 01.Block Diagram
- 02.SKU_table
- 03.Change Note
- 04.POWER SEQUENCE
- 05.CPU_DDR
- 06.CPU_Display
- 07.CPU_HDA/SDIO/EMMC/LPC /S
PI
- 08.CPU_USB3/USB2/PCIE/SATA
- 09.CPU_PMU/SVID/CLOCKS
- 10.CPU_SMBUS/I2C/CNVi
- 11.CPU_GPIO/JTAG
- 12.CPU_POWER
- 13.CPU_GND
- 14.CPU_STRAP
- 15.***
- 16.*****
- 17.
- 18.*****
- 19.LPDDR4_CH0_X32
- 20.LPDDR4_CH1_X32

Global Search

01.

02.

04.

05.

06.

07.

08.

09.

10.

11.

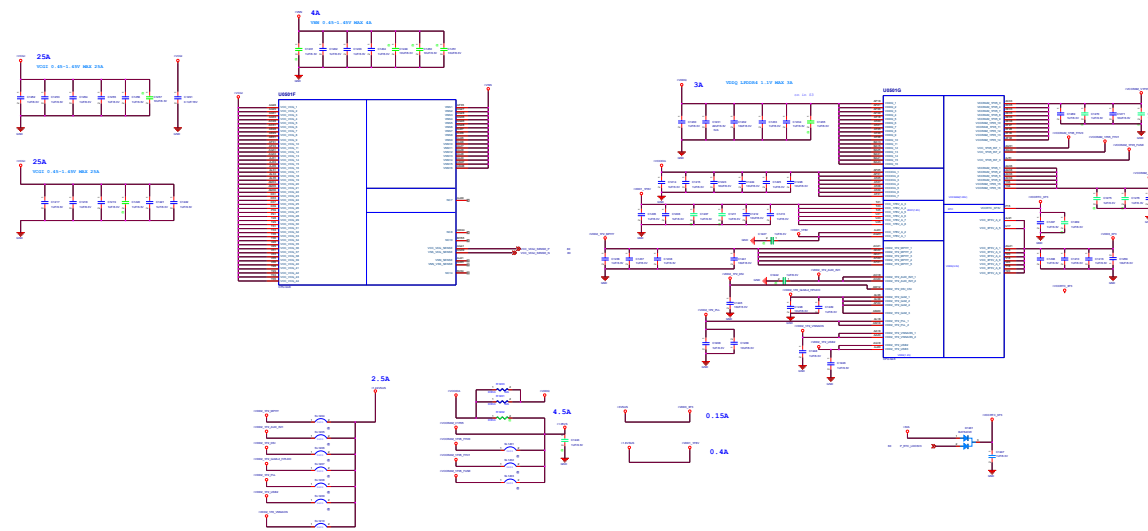
12.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

Global Search

13.

14.

19.

20.

24.

27.

28.

29.

30_

32.

36.

Toggle FullScreen

Pre Page

Next Page

MoveTo

18.*****

19.LPDDR4_CH0_X32

20.LPDDR4_CH1_X32

21.***

22.***

23.

24.WLAN

25.*****

26.

27.Debug

28.SPI ROM

29.KB_TP

30_ENE_KB902AQ

31.

32.RESET CIRCUIT

33.

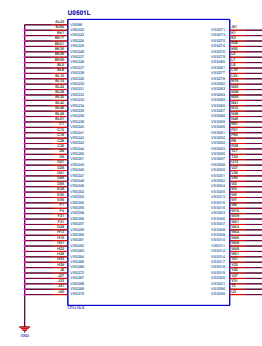
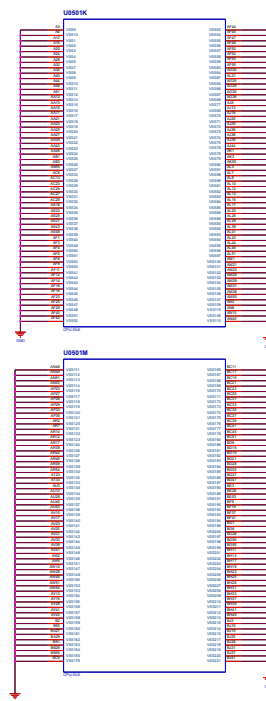
34.

35.

36.AUD-ALC3251

37.AUD-HEADPHONE JACK

22 Snooker



Schematic Page List

Hide

Global Search

13.

14.

19.

20.

24.

27.

28.

29.

30_

32.

36.

Toggle FullScreen

Pre Page

Next Page

MoveTo

18.*****

19.LPDDR4_CH0_X32

20.LPDDR4_CH1_X32

21.***

22.***

23.

24.WLAN

25.*****

26.

27.Debug

28.SPI ROM

29.KB_TP

30_ENE_KB902AQ

31.

32.RESET CIRCUIT

33.

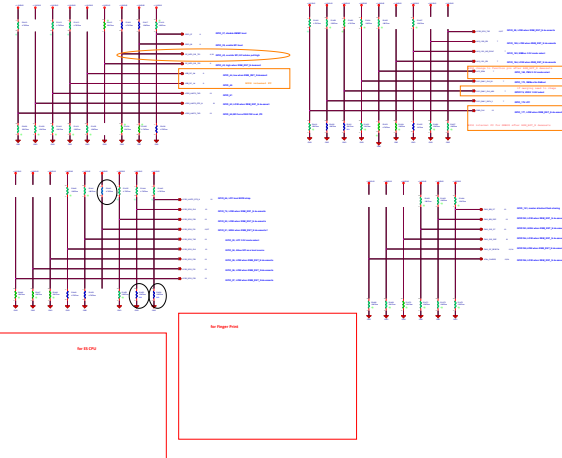
34.

35.

36.AUD-ALC3251

37.AUD-HEADPHONE JACK

22 Snorker

Table 2-27. Hardware Straps (Sheet 1 of 4)[illegible]Table 2-27. Hardware Steps (Sheet 2 of 2)[illegible]Table 2-27. Hardware Straps (Sheet 2 of 2)

SPR #	File Name	Revision	Issued	File Web Page/Description/Notes
SPR-135	SPR-135_001	0.0.0.0	200-7-1	SPR-135_001_001
SPR-137	SPR-137_001	0.0.0.0	200-7-1	SPR-137_001_001
SPR-138	SPR-138_001	0.0.0.0	200-7-1	SPR-138_001_001
SPR-139	SPR-139_001	0.0.0.0	200-7-1	SPR-139_001_001
SPR-140	SPR-140_001	0.0.0.0	200-7-1	SPR-140_001_001
SPR-141	SPR-141_001	0.0.0.0	200-7-1	SPR-141_001_001
SPR-142	SPR-142_001	0.0.0.0	200-7-1	SPR-142_001_001
SPR-143	SPR-143_001	0.0.0.0	200-7-1	SPR-143_001_001
SPR-144	SPR-144_001	0.0.0.0	200-7-1	SPR-144_001_001
SPR-145	SPR-145_001	0.0.0.0	200-7-1	SPR-145_001_001
SPR-146	SPR-146_001	0.0.0.0	200-7-1	SPR-146_001_001
SPR-147	SPR-147_001	0.0.0.0	200-7-1	SPR-147_001_001
SPR-148	SPR-148_001	0.0.0.0	200-7-1	SPR-148_001_001
SPR-149	SPR-149_001	0.0.0.0	200-7-1	SPR-149_001_001
SPR-150	SPR-150_001	0.0.0.0	200-7-1	SPR-150_001_001
SPR-151	SPR-151_001	0.0.0.0	200-7-1	SPR-151_001_001
SPR-152	SPR-152_001	0.0.0.0	200-7-1	SPR-152_001_001
SPR-153	SPR-153_001	0.0.0.0	200-7-1	SPR-153_001_001
SPR-154	SPR-154_001	0.0.0.0	200-7-1	SPR-154_001_001
SPR-155	SPR-155_001	0.0.0.0	200-7-1	SPR-155_001_001
SPR-156	SPR-156_001	0.0.0.0	200-7-1	SPR-156_001_001
SPR-157	SPR-157_001	0.0.0.0	200-7-1	SPR-157_001_001
SPR-158	SPR-158_001	0.0.0.0	200-7-1	SPR-158_001_001
SPR-159	SPR-159_001	0.0.0.0	200-7-1	SPR-159_001_001
SPR-160	SPR-160_001	0.0.0.0	200-7-1	SPR-160_001_001
SPR-161	SPR-161_001	0.0.0.0	200-7-1	SPR-161_001_001
SPR-162	SPR-162_001	0.0.0.0	200-7-1	SPR-162_001_001
SPR-163	SPR-163_001	0.0.0.0	200-7-1	SPR-163_001_001
SPR-164	SPR-164_001	0.0.0.0	200-7-1	SPR-164_001_001
SPR-165	SPR-165_001	0.0.0.0	200-7-1	SPR-165_001_001
SPR-166	SPR-166_001	0.0.0.0	200-7-1	SPR-166_001_001
SPR-167	SPR-167_001	0.0.0.0	200-7-1	SPR-167_001_001
SPR-168	SPR-168_001	0.0.0.0	200-7-1	SPR-168_001_001
SPR-169	SPR-169_001	0.0.0.0	200-7-1	SPR-169_001_001
SPR-170	SPR-170_001	0.0.0.0	200-7-1	SPR-170_001_001
SPR-171	SPR-171_001	0.0.0.0	200-7-1	SPR-171_001_001
SPR-172	SPR-172_001	0.0.0.0	200-7-1	SPR-172_001_001
SPR-173	SPR-173_001	0.0.0.0	200-7-1	SPR-173_001_001
SPR-174	SPR-174_001	0.0.0.0	200-7-1	SPR-174_001_001
SPR-175	SPR-175_001	0.0.0.0	200-7-1	SPR-175_001_001
SPR-176	SPR-176_001	0.0.0.0	200-7-1	SPR-176_001_001
SPR-177	SPR-177_001	0.0.0.0	200-7-1	SPR-177_001_001
SPR-178	SPR-178_001	0.0.0.0	200-7-1	SPR-178_001_001
SPR-179	SPR-179_001	0.0.0.0	200-7-1	SPR-179_001_001
SPR-180	SPR-180_001	0.0.0.0	200-7-1	SPR-180_001_001
SPR-181	SPR-181_001	0.0.0.0	200-7-1	SPR-181_001_001
SPR-182	SPR-182_001	0.0.0.0	200-7-1	SPR-182_001_001
SPR-183	SPR-183_001	0.0.0.0	200-7-1	SPR-183_001_001
SPR-184	SPR-184_001	0.0.0.0	200-7-1	SPR-184_001_001
SPR-185	SPR-185_001	0.0.0.0	200-7-1	SPR-185_001_001
SPR-186	SPR-186_001	0.0.0.0	200-7-1	SPR-186_001_001
SPR-187	SPR-187_001	0.0.0.0	200-7-1	SPR-187_001_001
SPR-188	SPR-188_001	0.0.0.0	200-7-1	SPR-188_001_001
SPR-189	SPR-189_001	0.0.0.0	200-7-1	SPR-1



Schematic Page List

Hide

Global Search

13.

14.

19.

20.

24.

27.

28.

29.

30_

32.

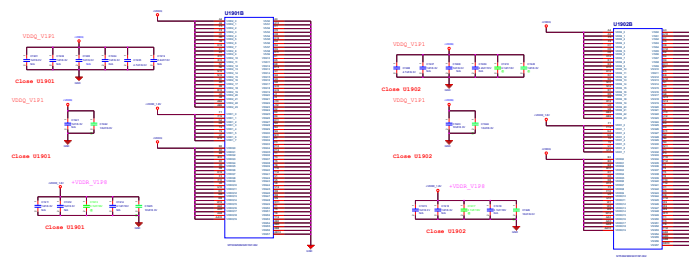
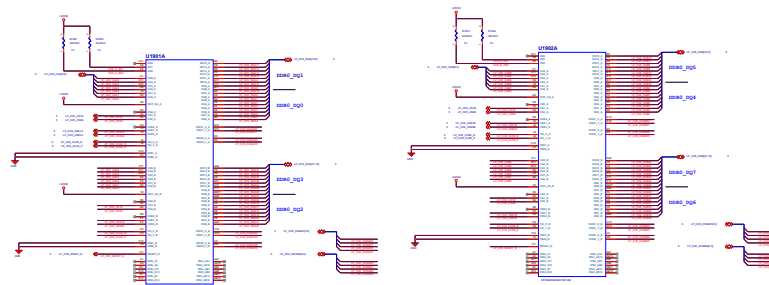
36.

Toggle FullScreen

Pre Page

Next Page

MoveTo



C/Boa	
10	10/10/10

Schematic Page List

Hide

Global Search

13.

14.

19.

20.

24.

27.

28.

29.

30_

32.

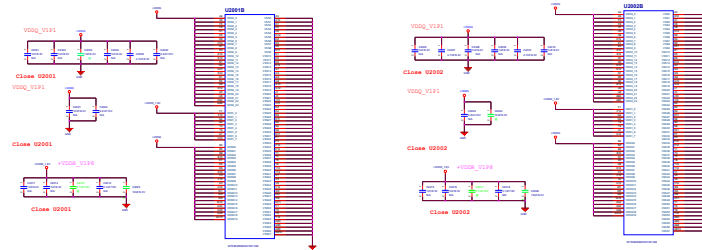
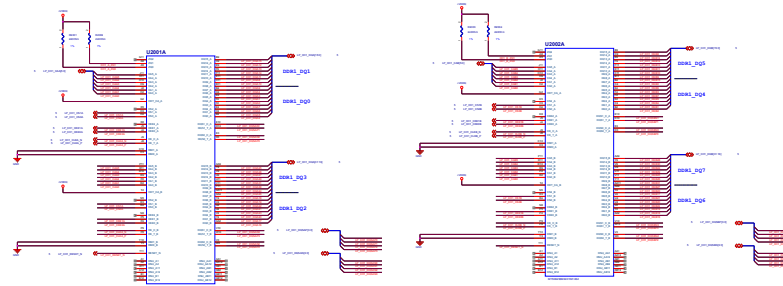
36.

Toggle FullScreen

Pre Page

Next Page

MoveTo [



Schematic Page List

Hide

Global Search

13.

14.

19.

20.

24.

27.

28.

29.

30_

32.

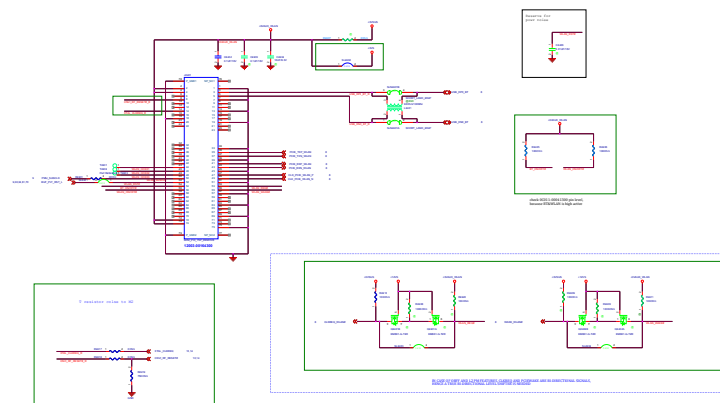
36.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

Global Search

13.

14.

19.

20.

24.

27.

28.

29.

30_

32.

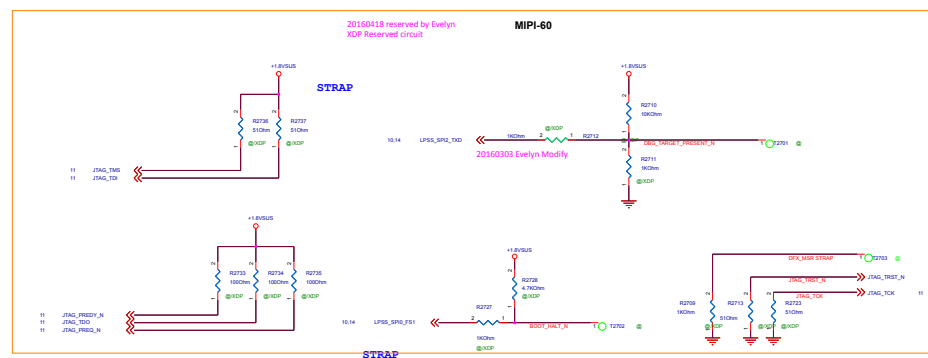
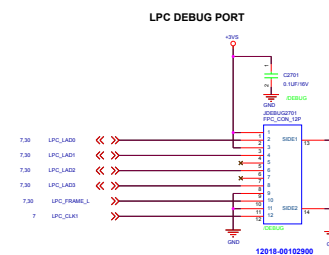
36.

Toggle FullScreen

Pre Page

Next Page

MoveTo



		Project Name		
		X540MB		
Title : Debug				
Size	Dept:	Engineer: Arian_Chiang		
0	NS2RD1EE1			

Schematic Page List

Hide

Global Search

13.

14.

19.

20.

24.

27.

28.

29.

30_

32.

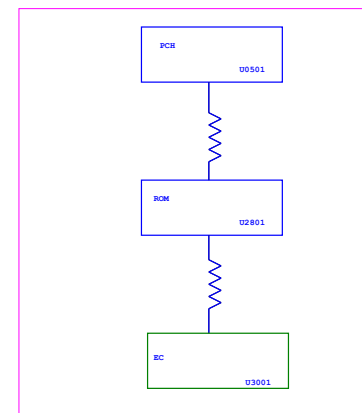
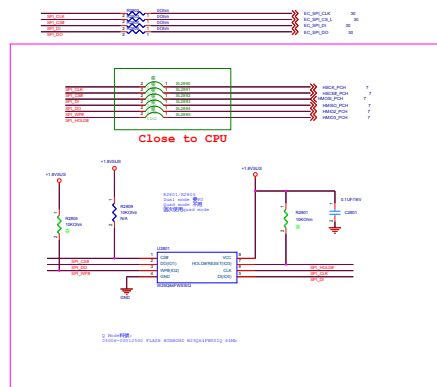
36.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

- 18.*****
- 19.LPDDR4_CH0_X32
- 20.LPDDR4_CH1_X32
- 21.***
- 22.***
- 23.
- 24.WLAN
- 25.*****
- 26.
- 27.Debug
- 28.SPI ROM
- 29.KB_TP
- 30_ENE_KB902AQ
- 31.
- 32.RESET CIRCUIT
- 33.
- 34.
- 35.
- 36.AUD-ALC3251
- 37.AUD-HEADPHONE JACK
- 38.Speaker

Global Search

13.

14.

19.

20.

24.

27.

28.

29.

30_

32.

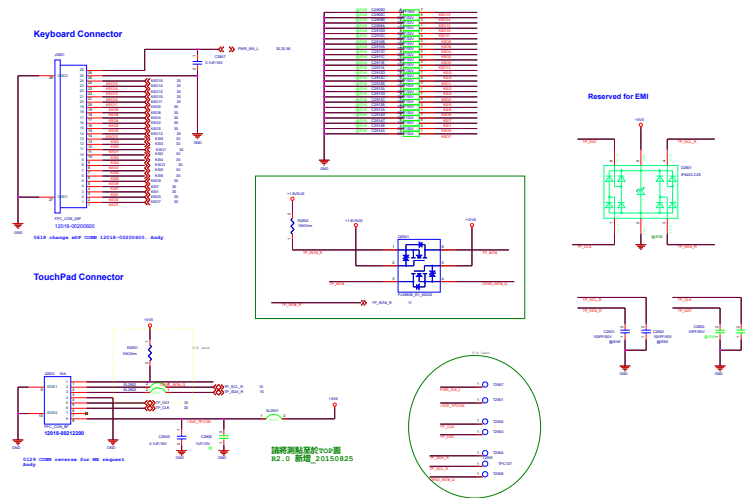
36.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

Global Search

13.

14.

19.

20.

24.

27.

28.

29.

30_

32.

36.

Toggle FullScreen

Pre Page

Next Page

MoveTo

18.*****

19.LPDDR4_CH0_X32

20.LPDDR4_CH1_X32

21.***

22.***

23.

24.WLAN

25.*****

26.

27.Debug

28.SPI ROM

29.KB TP

30_ENE_KB902AQ

31.

32.RESET CIRCUIT

33.

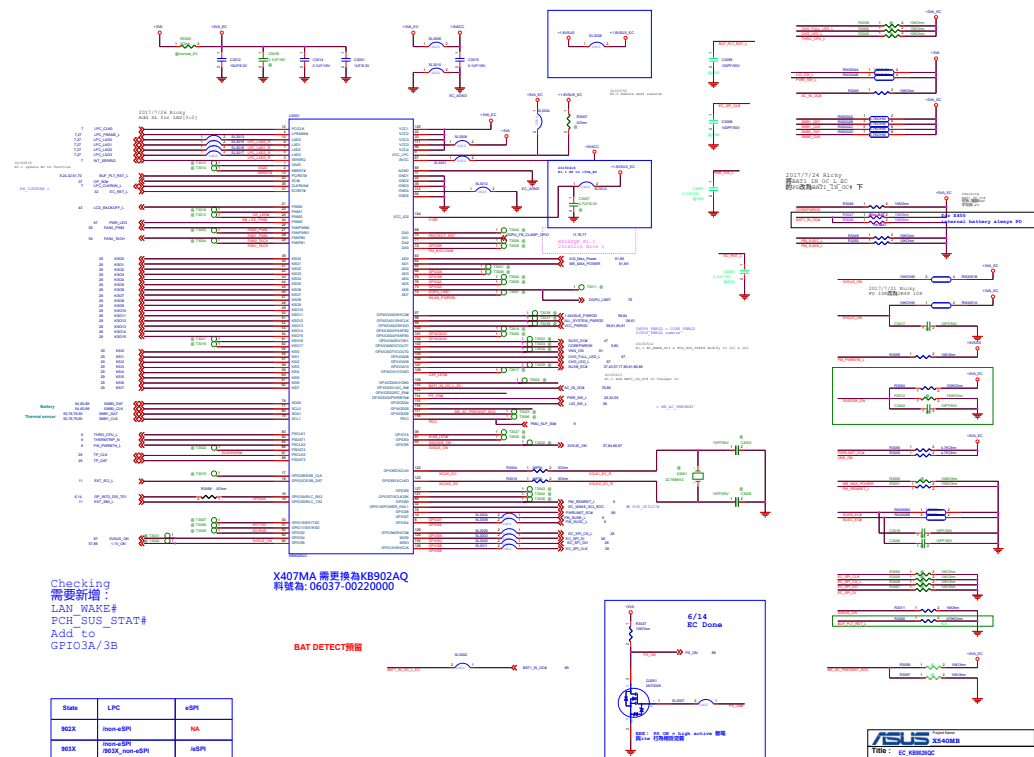
34.

35.

36.AUD-ALC3251

37.AUD-HEADPHONE JACK

22 Snooker



Schematic Page List

Hide

18.*****
19.LPDDR4_CH0_X32
20.LPDDR4_CH1_X32
21.***
22.***
23.
24.WLAN
25.*****
26.
27.Debug
28.SPI ROM
29.KB_TP
30_ENE_KB902AQ
31.
32.RESET CIRCUIT
33.
34.
35.
36.AUD-ALC3251
37.AUD-HEADPHONE JACK
38.Speaker

Global Search

13.

14.

19.

20.

24.

27.

28.

29.

30_

32.

36.

Toggle FullScreen

Pre Page

Next Page

MoveTo

Thermal Policy

Thermal Policy

ASUS

Z5400B

Table 1: Thermal Policy

Engineer: Arvin, Ching

Schematic Page List

Hide

Global Search

13.

14.

19.

20.

24.

27.

28.

29.

30_

32.

36.

Toggle FullScreen

Pre Page

Next Page

MoveTo

18.*****

19.LPDDR4_CH0_X32

20.LPDDR4_CH1_X32

21.***

22.***

23.

24.WLAN

25.*****

26.

27.Debug

28.SPI ROM

29.KB_TP

30_ENE_KB902AQ

31.

32.RESET CIRCUIT

33.

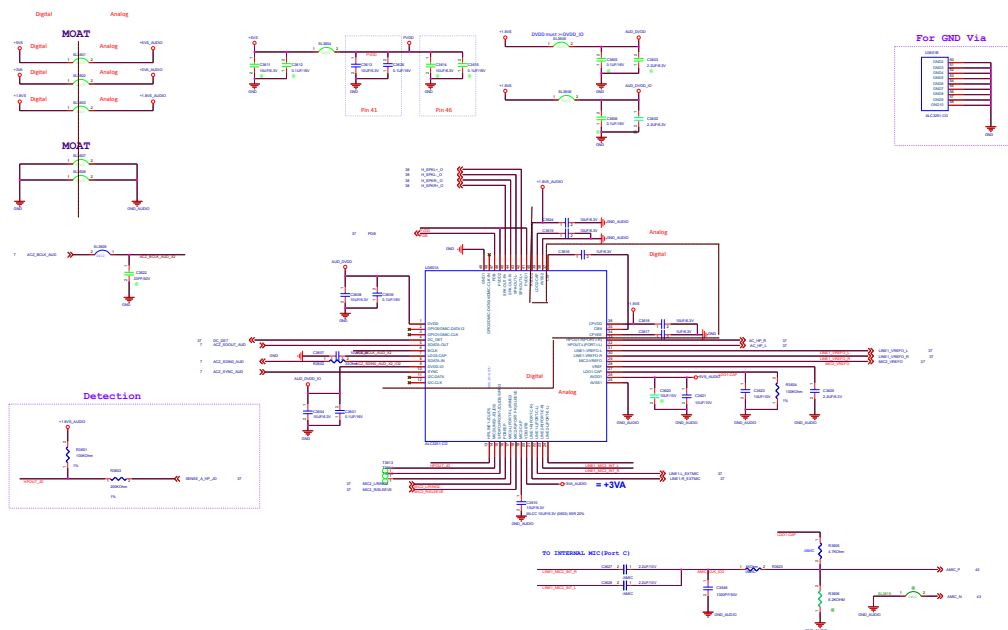
34.

35.

36.AUD-ALC3251

37.AUD-HEADPHONE JACK

22 Snooker



Schematic Page List

Hide

Global Search

37.

38.

39.

41.

43.

44.

47.

Toggle FullScreen

Pre Page

Next Page

MoveTo

28.SPI ROM

29.KB_TP

30_ENE_KB902AQ

31.

32.RESET CIRCUIT

33.

34.

35.

36.AUD-ALC3251

37.AUD-HEADPHONE JACK

38.Speaker

39.FPC Connector

40.

41.Card_Reader

42.

43.EDP

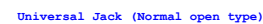
44.HDMI

45.

46.

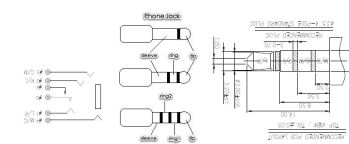
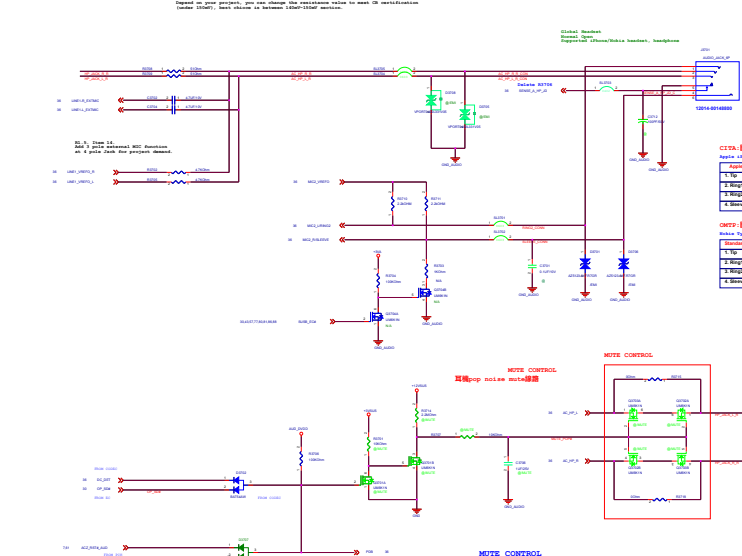
47.USB3_CON+2.0 CONN.

48.



H1.3. Item 12.
Add 4 pole broadcast jack rooms:
open type for project demand.

NI.4. Item 13.
Recommend the RF damping resistance 56 ohm for CE certification.
Depend on your project, you can change the resistance value to meet CE certification



CITA: 國際標準

Apple iPhone/iPad/小米 的 Phone Jack 定義

Apple	iPad (Stereo)	iPad (Stereo)	iPhone (Stereo)	iPad (HiFi)
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	Right channel	Right channel	Right channel	Right channel
3. Ring2	-	-	Ground	Ground
4. Sleeve	Ground	Ground	HiFi	Video

OMTP：國家標準

Kobin Type 的 Phone Jack 規格：

Standard	Mono	Stereo	Stereo + Mic	Audio + Video
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	-	Right channel	Right channel	Video
3. Ring2	-	-	Mic	Ground
4. Sleeve	Ground	Ground	Ground	Right channel



Schematic Page List

Hide

Global Search

37.

38.

39.

41.

43.

44.

47.

Toggle FullScreen

Pre Page

Next Page

MoveTo

28.SPI ROM

29.KB_TP

30_ENE_KB902AQ

31.

32.RESET CIRCUIT

33.

34.

35.

36.AUD-ALC3251

37.AUD-HEADPHONE JACK

38.Speaker

39.FPC Connector

40.

41.Card_Reader

42.

43.EDP

44.HDMI

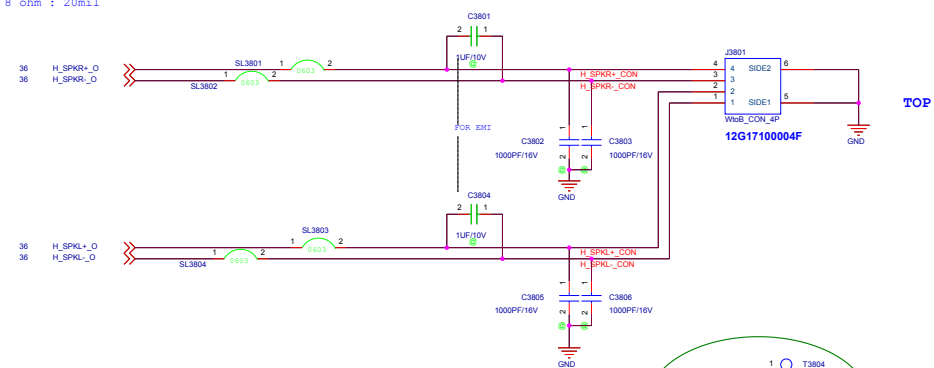
45.

46.


47.USB3_CON+2.0 CONN.

48.

```
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-RSpeaker
4 ohm : 40mil
Speaker 8 ohm : 20mil
```



請將測點至於TOP面
R2.0 新增 20150820

		Project Name		Rev
X540MB				1.0
Title : 38.Speaker				
Size A	Dept.: NB2RD1EE1		Engineer: Arian_Chiong	
Date: Friday, February 23, 2018	Shaw		18	of 90

Schematic Page List

Hide

- 28.SPI ROM
- 29.KB_TP
- 30._ENE_KB902AQ
- 31.
- 32.RESET CIRCUIT
- 33.
- 34.
- 35.
- 36.AUD-ALC3251
- 37.AUD-HEADPHONE JACK
- 38.Speaker
- 39.FPC Connector
- 40.
- 41.Card_Reader
- 42.
- 43.EDP
- 44.HDMI
- 45.
- 46.
- 47.USB3_CON+2.0 CONN.
- 48.

Global Search

37.

38.

39.

41.

43.

44.

47.

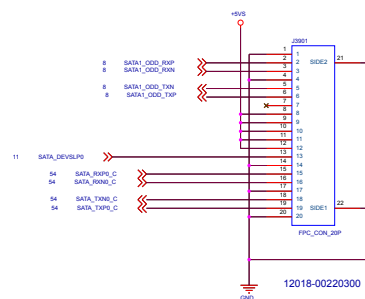
Toggle FullScreen

Pre Page

Next Page

MoveTo

FPC CONN : HDD & ODD



SATA PORT	SATA USAGE DEFAULT/OPTION
PORT 0	HDD
PORT 1	ODD

*Board Name:

		Title :	FPC CONN
Specification:		Engineer:	Arian_Chiang
Doc	Project Name	Rev	
B	X540MB	1.0	
Date: Friday, February 25, 2016		Sheet	30 of 60

Schematic Page List

Hide

- 28.SPI ROM
- 29.KB_TP
- 30_ENE_KB902AQ
- 31.
- 32.RESET CIRCUIT
- 33.
- 34.
- 35.
- 36.AUD-ALC3251
- 37.AUD-HEADPHONE JACK
- 38.Speaker
- 39.FPC Connector
- 40.
- 41.Card_Reader
- 42.
- 43.EDP
- 44.HDMI
- 45.
- 46.
- 47.USB3_CON+2.0 CONN.
- 48.

Global Search

37.

38.

39.

41.

43.

44.

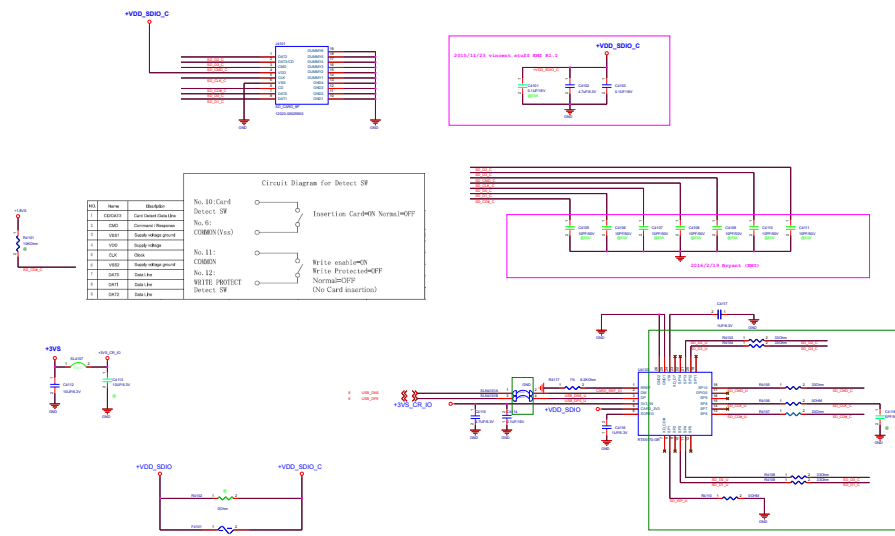
47.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

- 28.SPI ROM
- 29.KB_TP
- 30._ENE_KB902AQ
- 31.
- 32.RESET CIRCUIT
- 33.
- 34.
- 35.
- 36.AUD-ALC3251
- 37.AUD-HEADPHONE JACK
- 38.Speaker
- 39.FPC Connector
- 40.
- 41.Card_Reader
- 42.
- 43.EDP
- 44.HDMI
- 45.
- 46.
- 47.USB3_CON+2.0 CONN.
- 48.

Global Search

37.

38.

39.

41.

43.

44.

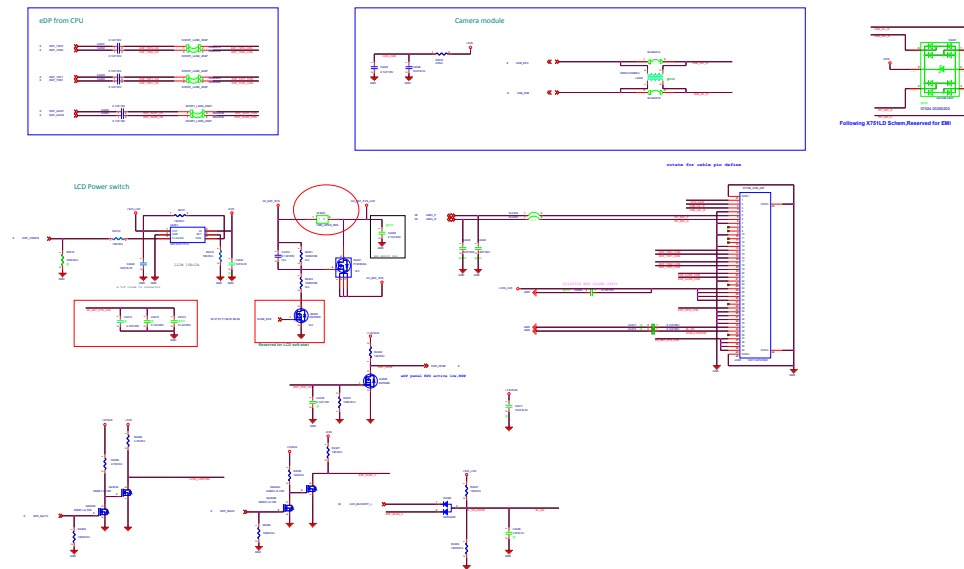
47.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

- 28.SPI ROM
- 29.KB_TP
- 30_ENE_KB902AQ
- 31.
- 32.RESET CIRCUIT
- 33.
- 34.
- 35.
- 36.AUD-ALC3251
- 37.AUD-HEADPHONE JACK
- 38.Speaker
- 39.FPC Connector
- 40.
- 41.Card_Reader
- 42.
- 43.EDP
- 44.HDMI
- 45.
- 46.
- 47.USB3_CON+2.0 CONN.
- 48.

Global Search

37.

38.

39.

41.

43.

44.

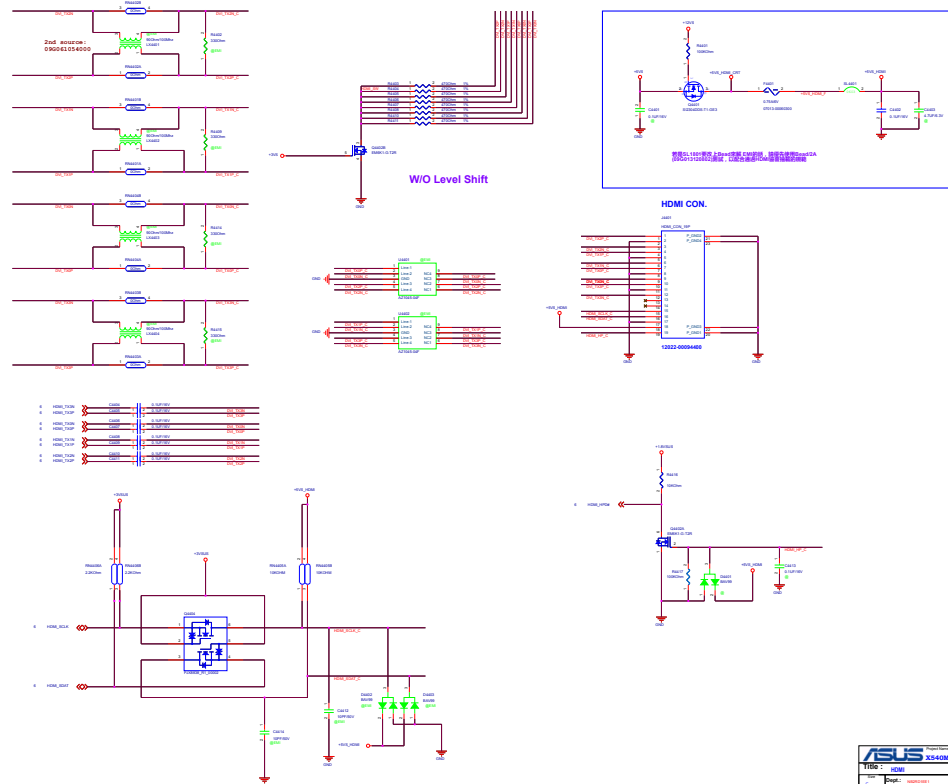
47.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

- 28.SPI ROM
- 29.KB_TP
- 30_ENE_KB902AQ
- 31.
- 32.RESET CIRCUIT
- 33.
- 34.
- 35.
- 36.AUD-ALC3251
- 37.AUD-HEADPHONE JACK
- 38.Speaker
- 39.FPC Connector
- 40.
- 41.Card_Reader
- 42.
- 43.EDP
- 44.HDMI
- 45.
- 46.
- 47.USB3_CON+2.0 CONN.
- 48.

Global Search

37.

38.

39.

41.

43.

44.

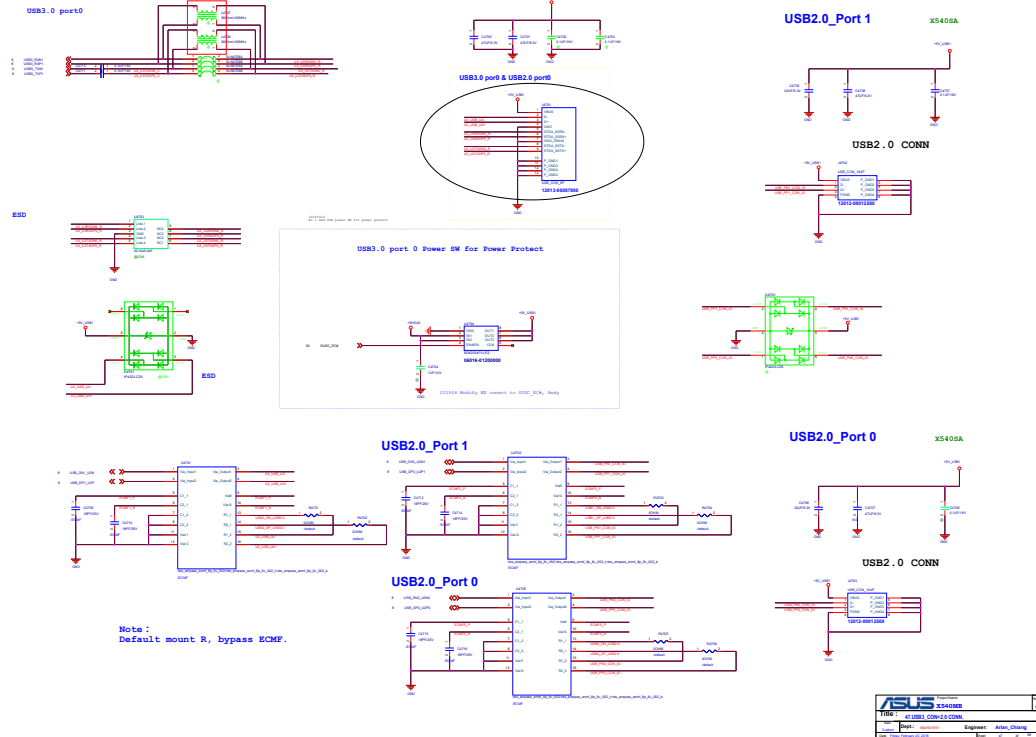
47.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

Global Search

60_

58.

57.

56.

54.

50.

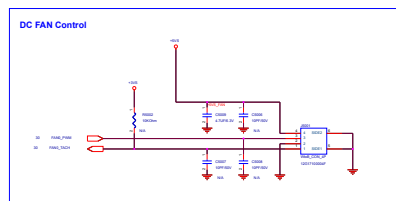
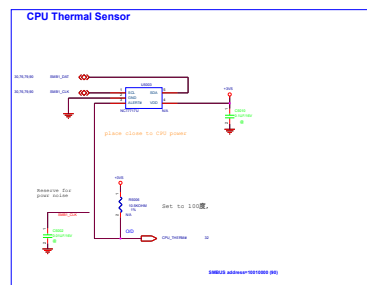
Toggle FullScreen

Pre Page

Next Page

MoveTo

Main Board



Schematic Page List

Hide

Global Search

60_

58.

57.

56.

54.

50.

Toggle FullScreen

Pre Page

Next Page

MoveTo

43.EDP

44.HDMI

45.

46.

47.USB3 CON+2.0 CONN.

48.

49.

50.Thermal Sensor & Fan

51.

52.

53.

54.SATA Redriver(ASM1467)

55.

56.Hall Sensor & Power Switch

57. Discharge

58.PWR_Protect

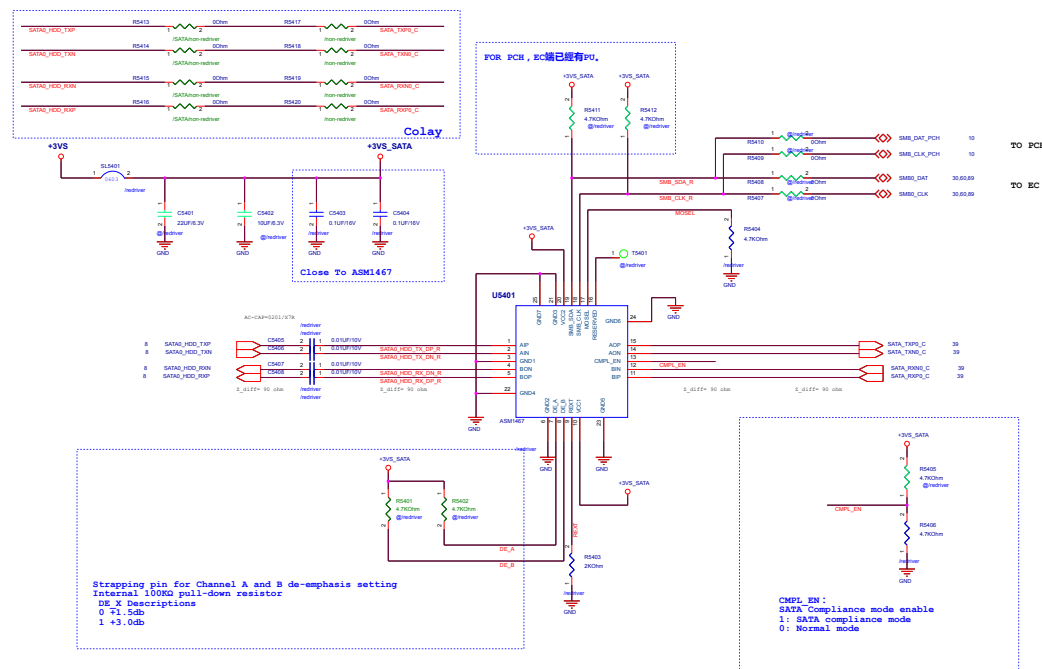
59.

60_DC & BAT IN

61.EMI

62.

63.



		Project Name	
		X540MB	
Title : 54.SATA Redriver(ASM1467)			
Size	Dept.: NS2PD1EE1	Engineer:	Arlian_Chiang
Date: Friday, February 25, 2016	Drawn:	By:	Rev: 00

Schematic Page List

Hide

- 43.EDP
- 44.HDMI
- 45.
- 46.
- 47.USB3_CON+2.0 CONN.
- 48.
- 49.
- 50.Thermal Sensor & Fan
- 51.
- 52.
- 53.
- 54.SATA Redriver(ASM1467)
- 55.
- 56.Hall Sensor & Power Switch
- 57.Discharge
- 58.PWR_Protect
- 59.
- 60_DC & BAT IN
- 61.EMI
- 62.
- 63.

Global Search

60_

58.

57.

56.

54.

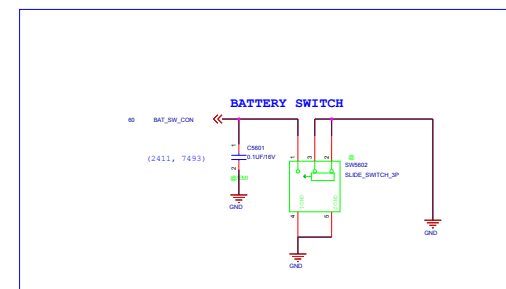
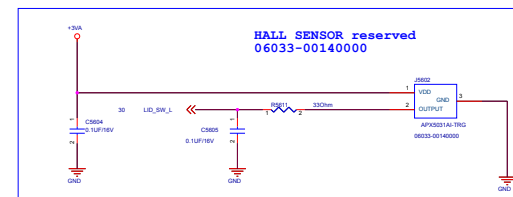
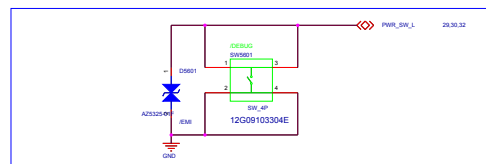
50.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Client Name:

ASUS		Title : Hall Sensor	
AS0621HE1		Engineer: Arian_Chiang	
Size	Project Name	Rev	
8	X540MB	1.0	
Date: Friday, February 23, 2018		Sheet	58 of 60

Schematic Page List

Hide

Global Search

60_

58.

57.

56.

54.

50.

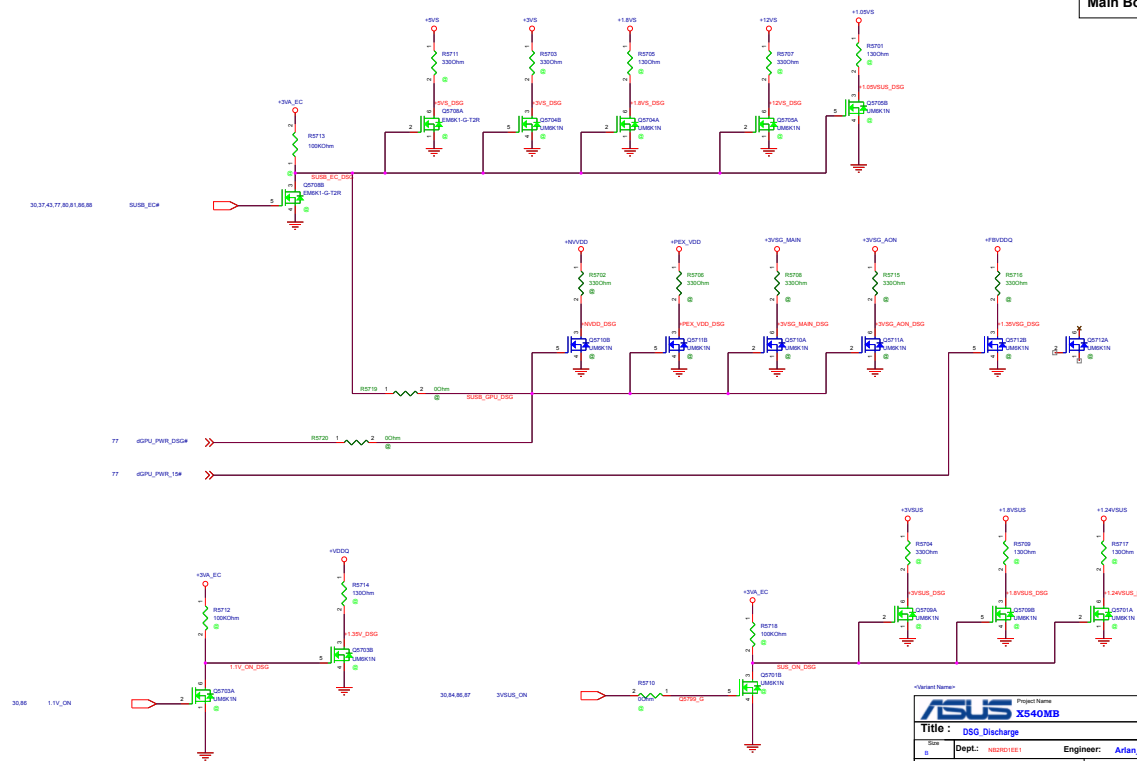
Toggle FullScreen


Pre Page

Next Page

MoveTo

Main Board



 Project Name X540MB	
Title : DSG Discharge	
Size Dept.: NB2RD1EE1	Engineer: Arlan_Chiang

Schematic Page List

Hide

- 43.EDP
- 44.HDMI
- 45.
- 46.
- 47.USB3_CON+2.0 CONN.
- 48.
- 49.
- 50.Thermal Sensor & Fan
- 51.
- 52.
- 53.
- 54.SATA Redriver(ASM1467)
- 55.
- 56.Hall Sensor & Power Switch
- 57.Discharge
- 58.PWR_Protect
- 59.
- 60_DC & BAT IN
- 61.EMI
- 62.
- 63.

Global Search

60_

58.

57.

56.

54.

50.

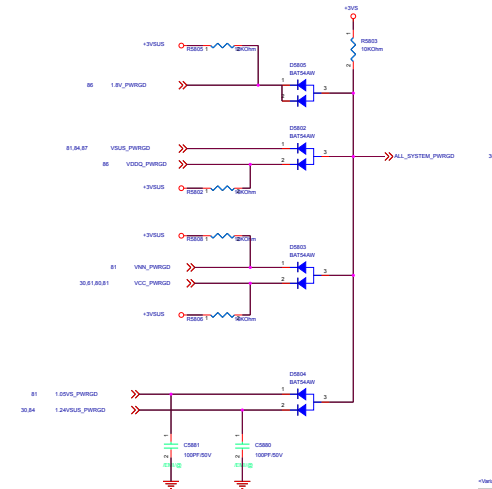
Toggle FullScreen

Pre Page

Next Page

MoveTo

POWER GOOD DETECTOR



ASUS		Project Name	Rev
X540MB			1.0
Title : PWR_Protect			
Drawn	Dept.:	ASUS	Engineer: Arlan_Chiang
Date: 2019.01.01		Drawn	50 of 50

Schematic Page List

Hide

- 43.EDP
- 44.HDMI
- 45.
- 46.
- 47.USB3_CON+2.0 CONN.
- 48.
- 49.
- 50.Thermal Sensor & Fan
- 51.
- 52.
- 53.
- 54.SATA Redriver(ASM1467)
- 55.
- 56.Hall Sensor & Power Switch
- 57.Discharge
- 58.PWR_Protect
- 59.
- 60_DC & BAT IN
- 61.EMI
- 62.
- 63.

Global Search

60_

58.

57.

56.

54.

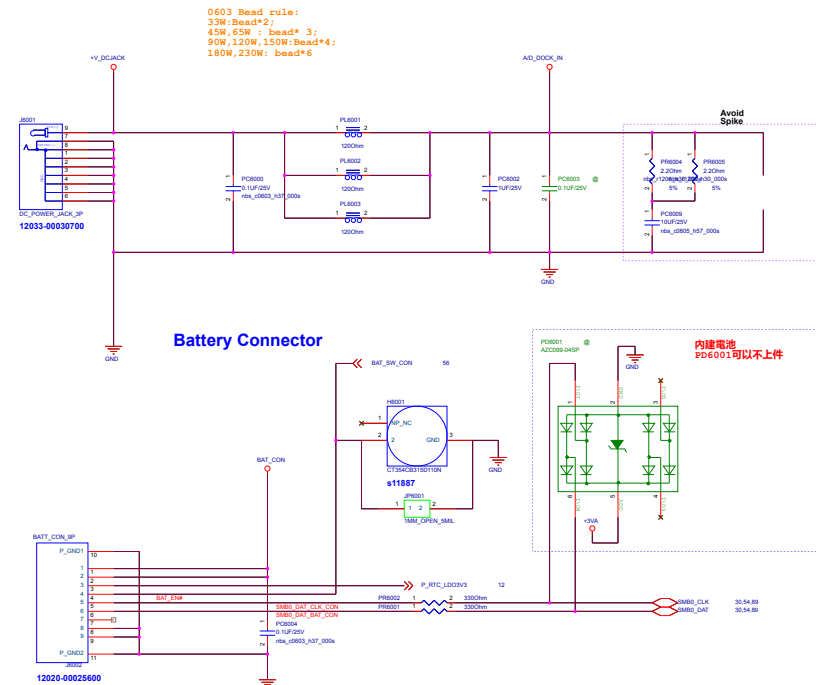
50.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Pin define should be checked after battery team confirm

ASUS		Project Name	Rev
X540MB			1.0
Title : 60_DC & BAT IN			
Dept:	NEEDYEE	Engineer:	Arian_Chiang
Date:	Friday, February 23, 2018	Sheet	85 of 89

Schematic Page List

Hide

- 43.EDP
- 44.HDMI
- 45.
- 46.
- 47.USB3_CON+2.0 CONN.
- 48.
- 49.
- 50.Thermal Sensor & Fan
- 51.
- 52.
- 53.
- 54.SATA Redriver(ASM1467)
- 55.
- 56.Hall Sensor & Power Switch
- 57.Discharge
- 58.PWR_Protect
- 59.
- 60_DC & BAT IN
- 61.EMI
- 62.
- 63.

Global Search

61.

60_

58.

57.

56.

54.

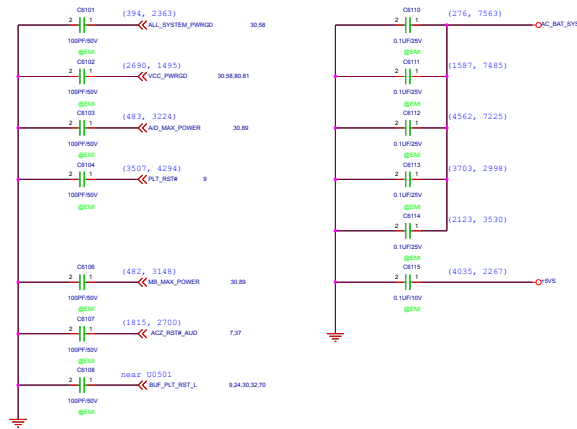
50.

Toggle FullScreen

Pre Page

Next Page

MoveTo



ASUS		Title : EMI	
ASUS		Engineer: Artan_Chiang	
Rev	Project Name	Rev	
C	X540MB	1.0	
Date: Friday, February 23, 2018		Print	01 of 00

Schematic Page List

Hide

60_DC & BAT IN
61.EMI
62.
63.
64.
65.ME_Conn & Skew Hole
66.
67.LED
68.
69.
70_VGA_nVIDIA_N16V/S_PCIE
71_VGA_nVIDIA_N16V/S_FB-IF
72_VGA_nVIDIA_N16V/S_FB-GD
DR5
73_VGA_nVIDIA_N16V/S_VDD
74_VGA_nVIDIA_N16V/S_DISPLA
Y
75_VGA_nVIDIA_N16V/S_ROM,X
TAL
76_VGA_nVIDIA_N16V/S_GPIO
77_VGA_nVIDIA_N16V/S_POWE

Global Search

79_

77_

76_

75_

74_

73_

72_

71_

70_

67.

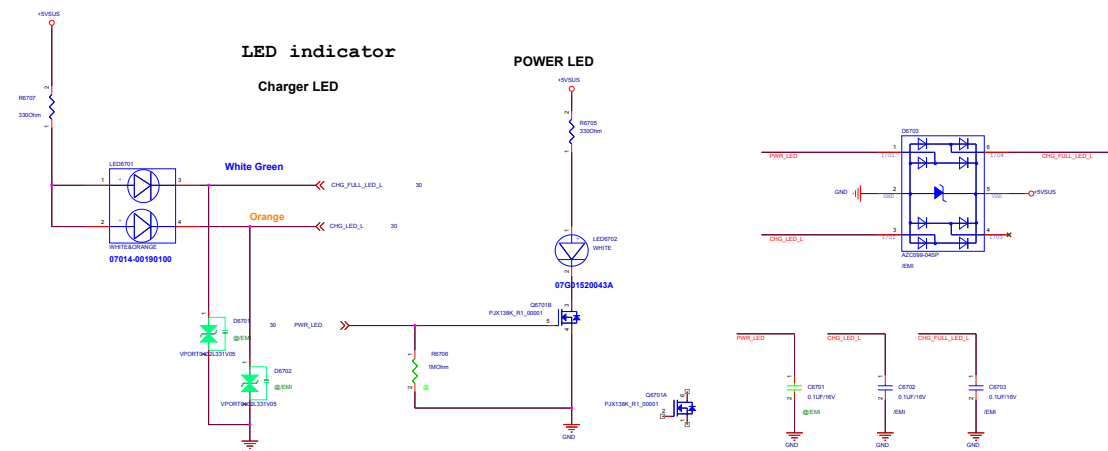
65.

Toggle FullScreen

Pre Page

Next Page

MoveTo



這3根 LED 信號 接 ENE 待確認 (1103/1805)

Schematic Page List

Hide

Global Search

79_

77_

76_

75_

74_

73_

72_

71_

70_

67.

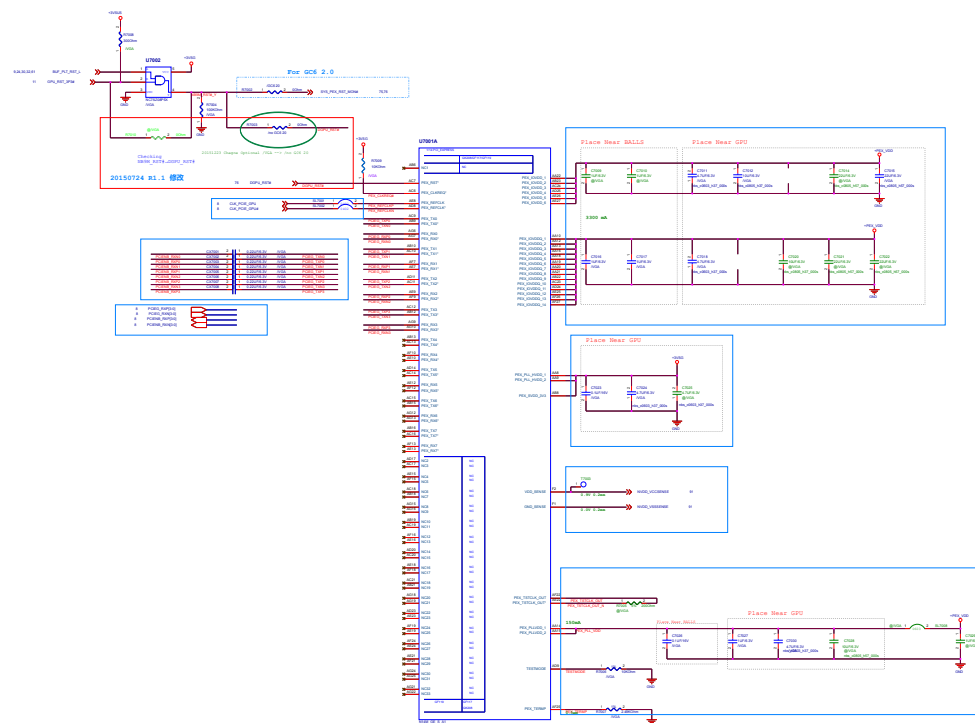
65.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

60_DC & BAT IN

61.EMI

62.

63.

64.

65.ME_Conn & Skew Hole

66.

67.LED

68.

69.

70_VGA_nVIDIA_N16V/S_PCIE

71_VGA_nVIDIA_N16V/S_FB-IF

72_VGA_nVIDIA_N16V/S_FB-GD
DR5

73_VGA_nVIDIA_N16V/S_VDD

74_VGA_nVIDIA_N16V/S_DISPLA
Y75_VGA_nVIDIA_N16V/S_ROM,X
TAL

76_VGA_nVIDIA_N16V/S_GPIO

77_VGA_nVIDIA_N16V/S_POWE

Global Search

79_

77_

76_

75_

74_

73_

72_

71_

70_

67.

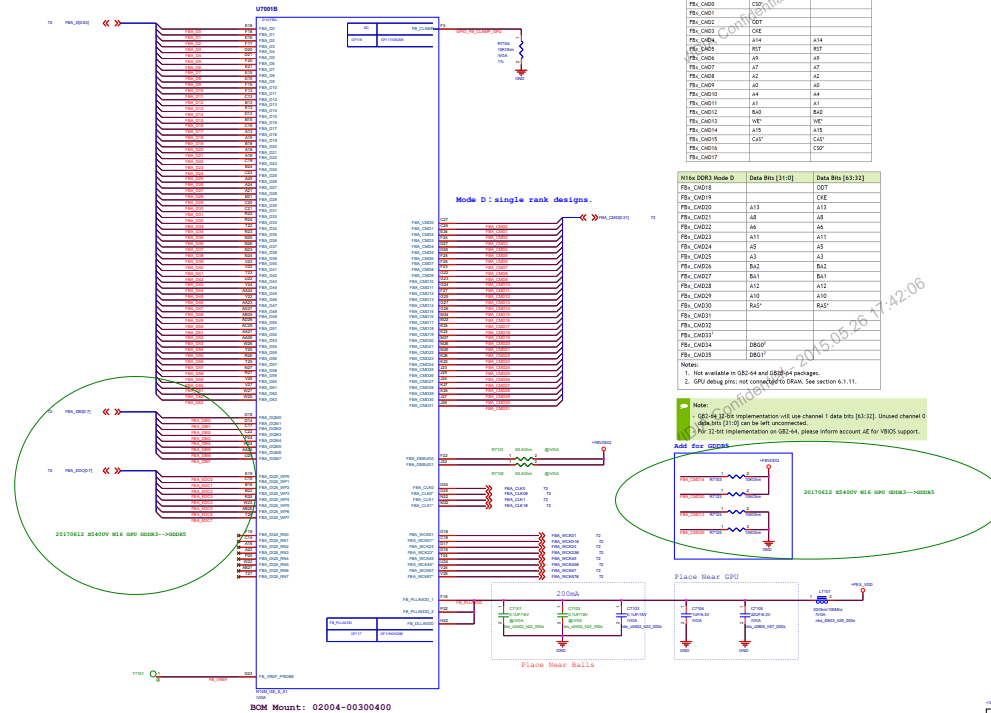
65.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

60_DC & BAT IN
61.EMI
62.
63.
64.
65.ME_Conn & Skew Hole
66.
67.LED
68.
69.
70_VGA_nVIDIA_N16V/S_PCIE
71_VGA_nVIDIA_N16V/S_FB-IF
72_VGA_nVIDIA_N16V/S_FB-GD
DR5
73_VGA_nVIDIA_N16V/S_VDD
74_VGA_nVIDIA_N16V/S_DISPLA
Y
75_VGA_nVIDIA_N16V/S_ROM,X
TAL
76_VGA_nVIDIA_N16V/S_GPIO
77_VGA_nVIDIA_N16V/S_POWE

Global Search

79_

77_

76_

75_

74_

73_

72_

71_

70_

67.

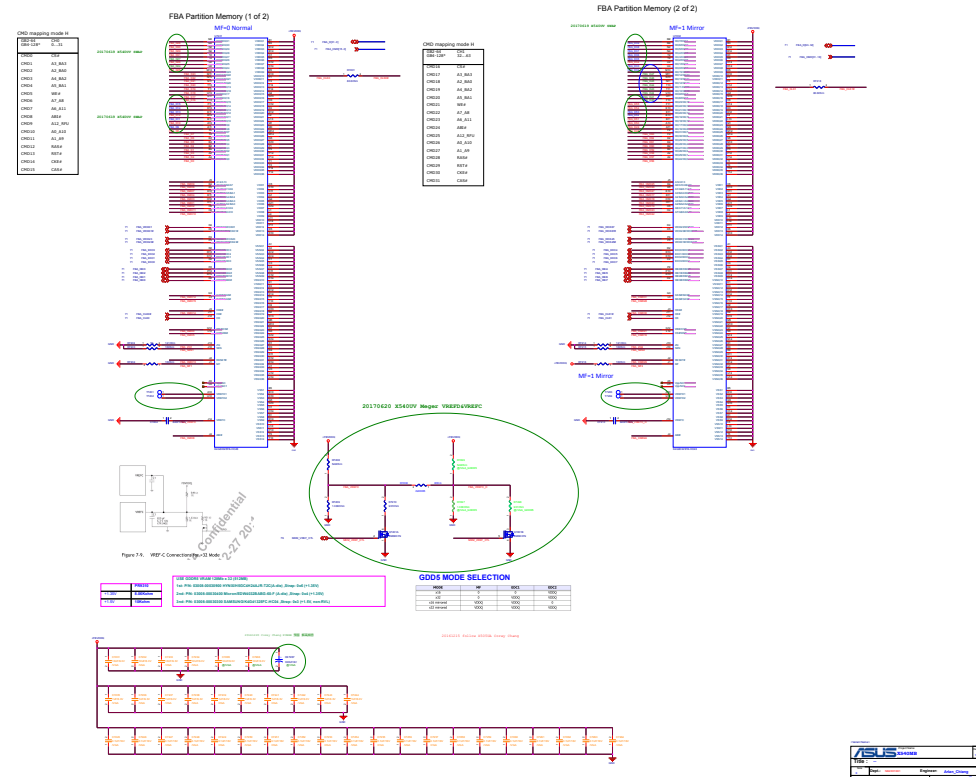
65.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

Global Search

79_

77_

76_

75_

74_

73_

72_

71_

70_

67.

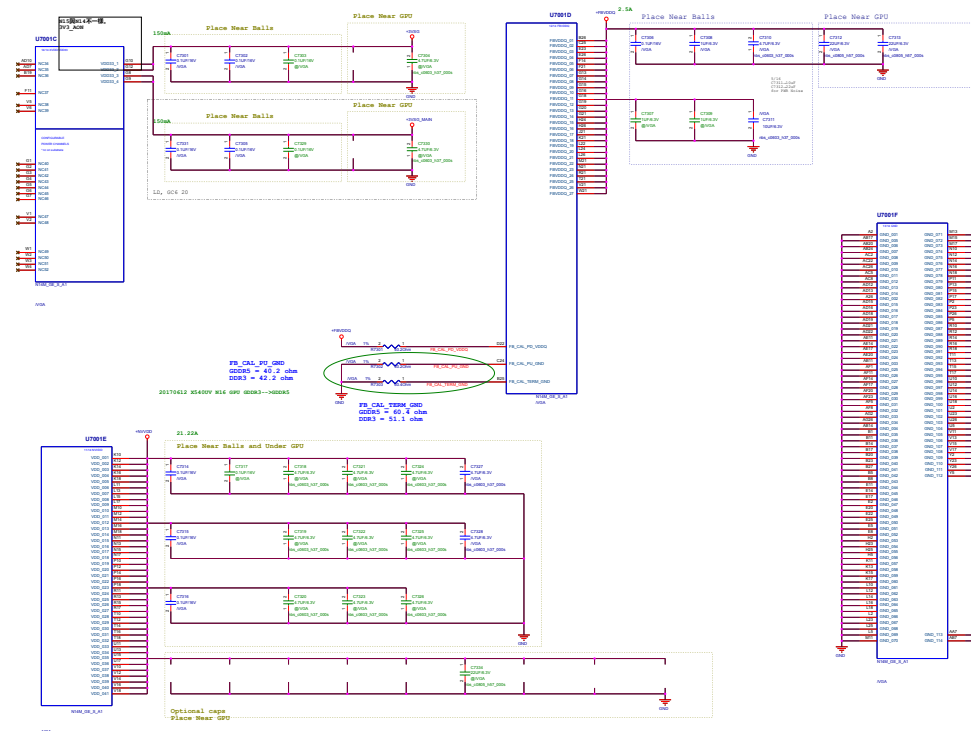
65.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

Global Search

79_

77_

76_

75_

74_

73_

72_

71_

70_

67.

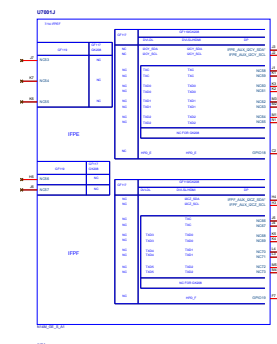
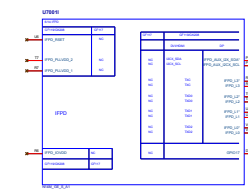
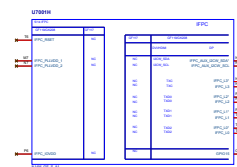
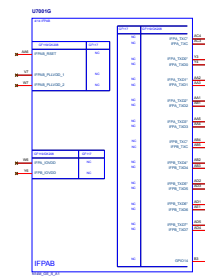
65.

Toggle FullScreen

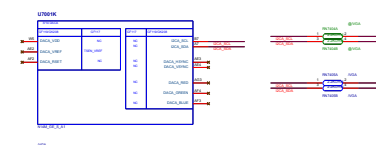
Pre Page

Next Page

MoveTo



CRT



Schematic Page List

Hide

60_DC & BAT IN
61.EMI
62.
63.
64.
65.ME_Conn & Skew Hole
66.
67.LED
68.
69.
70_VGA_nVIDIA_N16V/S_PCIE
71_VGA_nVIDIA_N16V/S_FB-IF
72_VGA_nVIDIA_N16V/S_FB-GD
DR5

73_VGA_nVIDIA_N16V/S_VDD
74_VGA_nVIDIA_N16V/S_DISPLA
Y
75_VGA_nVIDIA_N16V/S_ROM,X
TAL
76_VGA_nVIDIA_N16V/S_GPIO
77_VGA_nVIDIA_N16V/S_POWE

Global Search

79_

77_

76_

75_

74_

73_

72_

71_

70_

67.

65.

Toggle FullScreen

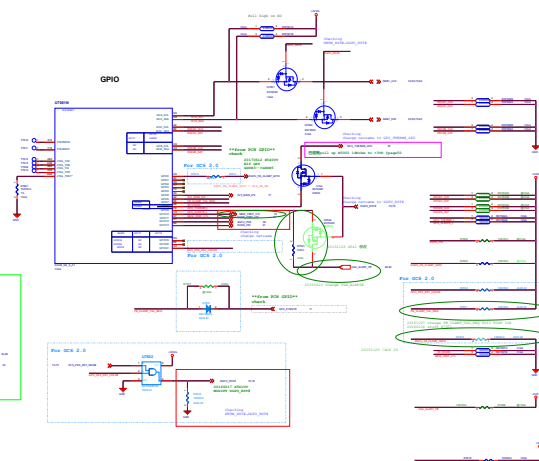
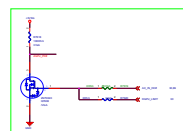
Pre Page

Next Page

MoveTo

Table 12-1: G520-M and G540-M GPIO Description

Pin	Signal Function	IO	Pin Description	Recommended Default
GPIO0	GPIO0	I/O	GPIO0	GPIO0
GPIO1	GPIO1	I/O	GPIO1	GPIO1
GPIO2	GPIO2	I/O	GPIO2	GPIO2
GPIO3	GPIO3	I/O	GPIO3	GPIO3
GPIO4	GPIO4	I/O	GPIO4	GPIO4
GPIO5	GPIO5	I/O	GPIO5	GPIO5
GPIO6	GPIO6	I/O	GPIO6	GPIO6
GPIO7	GPIO7	I/O	GPIO7	GPIO7
GPIO8	GPIO8	I/O	GPIO8	GPIO8
GPIO9	GPIO9	I/O	GPIO9	GPIO9
GPIO10	GPIO10	I/O	GPIO10	GPIO10
GPIO11	GPIO11	I/O	GPIO11	GPIO11
GPIO12	GPIO12	I/O	GPIO12	GPIO12
GPIO13	GPIO13	I/O	GPIO13	GPIO13
GPIO14	GPIO14	I/O	GPIO14	GPIO14
GPIO15	GPIO15	I/O	GPIO15	GPIO15
GPIO16	GPIO16	I/O	GPIO16	GPIO16
GPIO17	GPIO17	I/O	GPIO17	GPIO17
GPIO18	GPIO18	I/O	GPIO18	GPIO18
GPIO19	GPIO19	I/O	GPIO19	GPIO19
GPIO20	GPIO20	I/O	GPIO20	GPIO20
GPIO21	GPIO21	I/O	GPIO21	GPIO21
GPIO22	GPIO22	I/O	GPIO22	GPIO22
GPIO23	GPIO23	I/O	GPIO23	GPIO23
GPIO24	GPIO24	I/O	GPIO24	GPIO24
GPIO25	GPIO25	I/O	GPIO25	GPIO25
GPIO26	GPIO26	I/O	GPIO26	GPIO26
GPIO27	GPIO27	I/O	GPIO27	GPIO27
GPIO28	GPIO28	I/O	GPIO28	GPIO28
GPIO29	GPIO29	I/O	GPIO29	GPIO29
GPIO30	GPIO30	I/O	GPIO30	GPIO30
GPIO31	GPIO31	I/O	GPIO31	GPIO31
GPIO32	GPIO32	I/O	GPIO32	GPIO32
GPIO33	GPIO33	I/O	GPIO33	GPIO33
GPIO34	GPIO34	I/O	GPIO34	GPIO34
GPIO35	GPIO35	I/O	GPIO35	GPIO35
GPIO36	GPIO36	I/O	GPIO36	GPIO36
GPIO37	GPIO37	I/O	GPIO37	GPIO37
GPIO38	GPIO38	I/O	GPIO38	GPIO38
GPIO39	GPIO39	I/O	GPIO39	GPIO39
GPIO40	GPIO40	I/O	GPIO40	GPIO40
GPIO41	GPIO41	I/O	GPIO41	GPIO41
GPIO42	GPIO42	I/O	GPIO42	GPIO42
GPIO43	GPIO43	I/O	GPIO43	GPIO43
GPIO44	GPIO44	I/O	GPIO44	GPIO44
GPIO45	GPIO45	I/O	GPIO45	GPIO45
GPIO46	GPIO46	I/O	GPIO46	GPIO46
GPIO47	GPIO47	I/O	GPIO47	GPIO47
GPIO48	GPIO48	I/O	GPIO48	GPIO48
GPIO49	GPIO49	I/O	GPIO49	GPIO49
GPIO50	GPIO50	I/O	GPIO50	GPIO50
GPIO51	GPIO51	I/O	GPIO51	GPIO51
GPIO52	GPIO52	I/O	GPIO52	GPIO52
GPIO53	GPIO53	I/O	GPIO53	GPIO53
GPIO54	GPIO54	I/O	GPIO54	GPIO54
GPIO55	GPIO55	I/O	GPIO55	GPIO55
GPIO56	GPIO56	I/O	GPIO56	GPIO56
GPIO57	GPIO57	I/O	GPIO57	GPIO57
GPIO58	GPIO58	I/O	GPIO58	GPIO58
GPIO59	GPIO59	I/O	GPIO59	GPIO59
GPIO60	GPIO60	I/O	GPIO60	GPIO60
GPIO61	GPIO61	I/O	GPIO61	GPIO61
GPIO62	GPIO62	I/O	GPIO62	GPIO62
GPIO63	GPIO63	I/O	GPIO63	GPIO63
GPIO64	GPIO64	I/O	GPIO64	GPIO64
GPIO65	GPIO65	I/O	GPIO65	GPIO65
GPIO66	GPIO66	I/O	GPIO66	GPIO66
GPIO67	GPIO67	I/O	GPIO67	GPIO67
GPIO68	GPIO68	I/O	GPIO68	GPIO68
GPIO69	GPIO69	I/O	GPIO69	GPIO69
GPIO70	GPIO70	I/O	GPIO70	GPIO70
GPIO71	GPIO71	I/O	GPIO71	GPIO71
GPIO72	GPIO72	I/O	GPIO72	GPIO72
GPIO73	GPIO73	I/O	GPIO73	GPIO73
GPIO74	GPIO74	I/O	GPIO74	GPIO74
GPIO75	GPIO75	I/O	GPIO75	GPIO75
GPIO76	GPIO76	I/O	GPIO76	GPIO76
GPIO77	GPIO77	I/O	GPIO77	GPIO77
GPIO78	GPIO78	I/O	GPIO78	GPIO78
GPIO79	GPIO79	I/O	GPIO79	GPIO79
GPIO80	GPIO80	I/O	GPIO80	GPIO80
GPIO81	GPIO81	I/O	GPIO81	GPIO81
GPIO82	GPIO82	I/O	GPIO82	GPIO82
GPIO83	GPIO83	I/O	GPIO83	GPIO83
GPIO84	GPIO84	I/O	GPIO84	GPIO84
GPIO85	GPIO85	I/O	GPIO85	GPIO85
GPIO86	GPIO86	I/O	GPIO86	GPIO86
GPIO87	GPIO87	I/O	GPIO87	GPIO87
GPIO88	GPIO88	I/O	GPIO88	GPIO88
GPIO89	GPIO89	I/O	GPIO89	GPIO89
GPIO90	GPIO90	I/O	GPIO90	GPIO90
GPIO91	GPIO91	I/O	GPIO91	GPIO91
GPIO92	GPIO92	I/O	GPIO92	GPIO92
GPIO93	GPIO93	I/O	GPIO93	GPIO93
GPIO94	GPIO94	I/O	GPIO94	GPIO94
GPIO95	GPIO95	I/O	GPIO95	GPIO95
GPIO96	GPIO96	I/O	GPIO96	GPIO96
GPIO97	GPIO97	I/O	GPIO97	GPIO97
GPIO98	GPIO98	I/O	GPIO98	GPIO98
GPIO99	GPIO99	I/O	GPIO99	GPIO99



Schematic Page List

Hide

Global Search

79

77

76

75

74

73

72

71

70

67.

65.

Toggle FullScreen

Pre Page

Next Page

MoveTo

9

60_DC & BAT IN

61.EMI

62.

63.

64.

65.ME_Conn & Skew Hole

66.

67.LED

68.

69.

70_VGA_nVIDIA_N16V/S_PCIE

71 VGA nVIDIA N16V/S FB-IF

72_VGA_nVIDIA_N16V/S_FB-GD
DR5

73_VGA_nVIDIA_N16V/S_VDD

74_VGA_nVIDIA_N16V/S_DISPLAY

75_VGA_nVIDIA_N16V/S_ROM,X
TAL

76_VGA_nVIDIA_N16V/S_GPIO

77 VGA nVIDIA N16V/S POWE

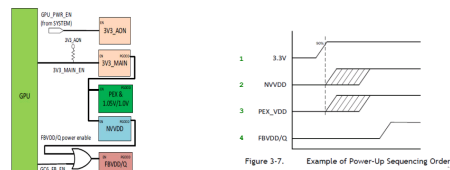
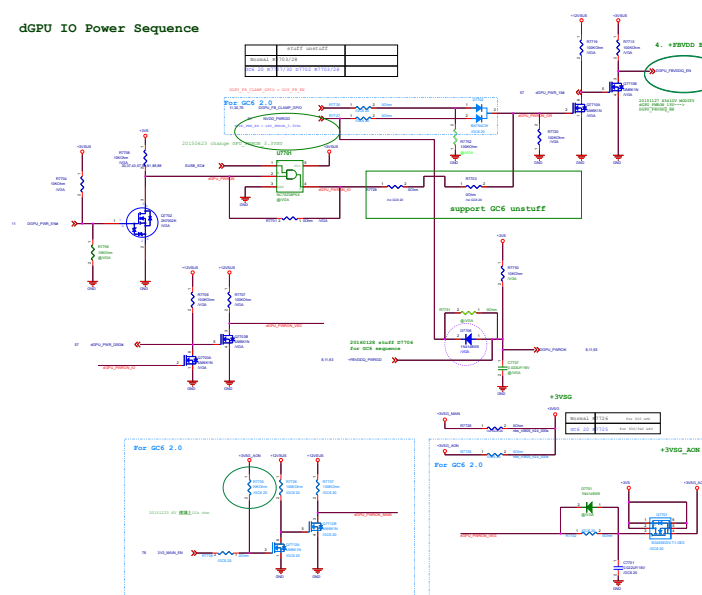
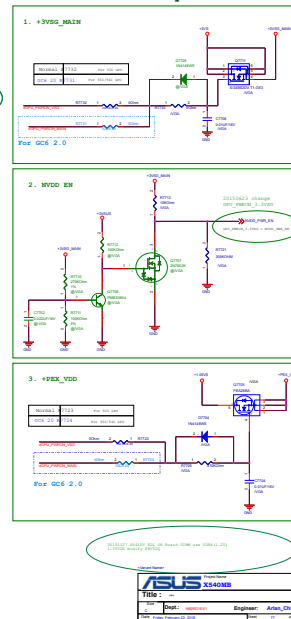


Figure 3-7. Example of Power-Up Sequencing Order

dGPU IO Power Sequence



dGPU Core Power Sequence



Schematic Page List

Hide

60_DC & BAT IN

61.EMI

62.

63.

64.

65.ME_Conn & Skew Hole

66.

67.LED

68.

69.

70_VGA_nVIDIA_N16V/S_PCIE

71_VGA_nVIDIA_N16V/S_FB-IF

72_VGA_nVIDIA_N16V/S_FB-GD DR5

73_VGA_nVIDIA_N16V/S_VDD

74_VGA_nVIDIA_N16V/S_DISPLA Y

75_VGA_nVIDIA_N16V/S_ROM,X TAL

76_VGA_nVIDIA_N16V/S_GPIO

77_VGA_nVIDIA_N16V/S_POWE

Global Search

79_

77_

76_

75_

74_

73_

72_

71_

70_

67.

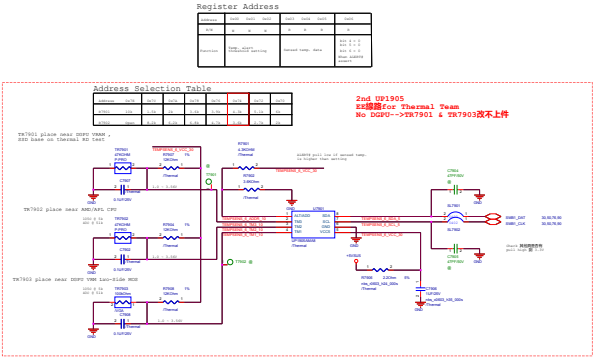
65.

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

~~TF_VOR_IVIDIA_INOVVO_DISPLAY~~
Y

75_VGA_nVIDIA_N16V/S_ROM,X
TAL

76_VGA_nVIDIA_N16V/S_GPIO

77_VGA_nVIDIA_N16V/S_POWE
R

78.

79_PROTECTION_2nd UP1905

80 PW APL VCGI P

81_PW_APL_VCGI/MNN_P

82_PW_***

83_PW_

84_PW_+1.8VSUS/+1.24VSUS

85_PW_***

86_PW_+VDDQ/+VTT/+1.8V

87_PW_+3VSUS/+5VSUS

88 PW LOAD SWITCH

89.PW_CHARGER(SN2867RUYR)
P

90_PW_PROTECTION(w/o counte
r)

91_PW_+NVVDD (RT8820A)

Global Search

99_

93_

91_

90_

89.

88_

87_

86_

84_

81_

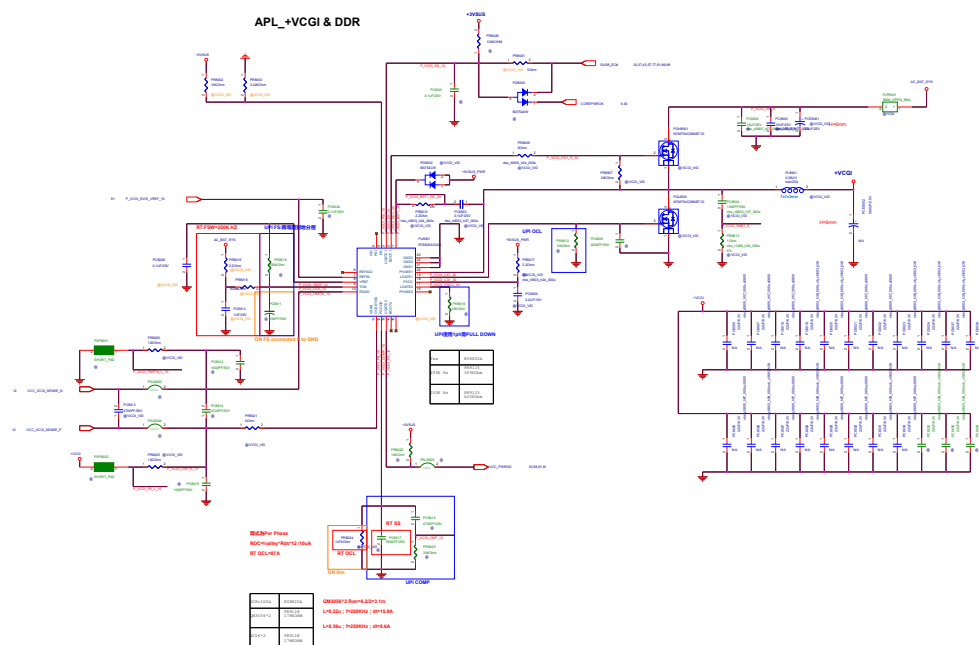
80_

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

~~TF_VOR_NVIDIA_INTX70_DISPLAY~~
Y

75_VGA_nVIDIA_N16V/S_ROM,X
TAL

76_VGA_nVIDIA_N16V/S_GPIO

77_VGA_nVIDIA_N16V/S_POWE
R

78.

79_PROTECTION_2nd UP1905

80 PW APL VCGI P

81_PW_APL_VCGI/VNN_P

82_PW_***

83_PW_

84_PW_+1.8VSUS/+1.24VSUS

85_PW_***

86_PW_+VDDQ/+VTT/+1.8V

87_PW_+3VSUS/+5VSUS

88 PW LOAD SWITCH

89.PW_CHARGER(SN2867RUYR)
P

90_PW_PROTECTION(w/o counte
r)

91_PW_+NVVDD (RT8820A)

Global Search

99_

93_

91_

90_

89.

88_

87_

86_

84_

81_

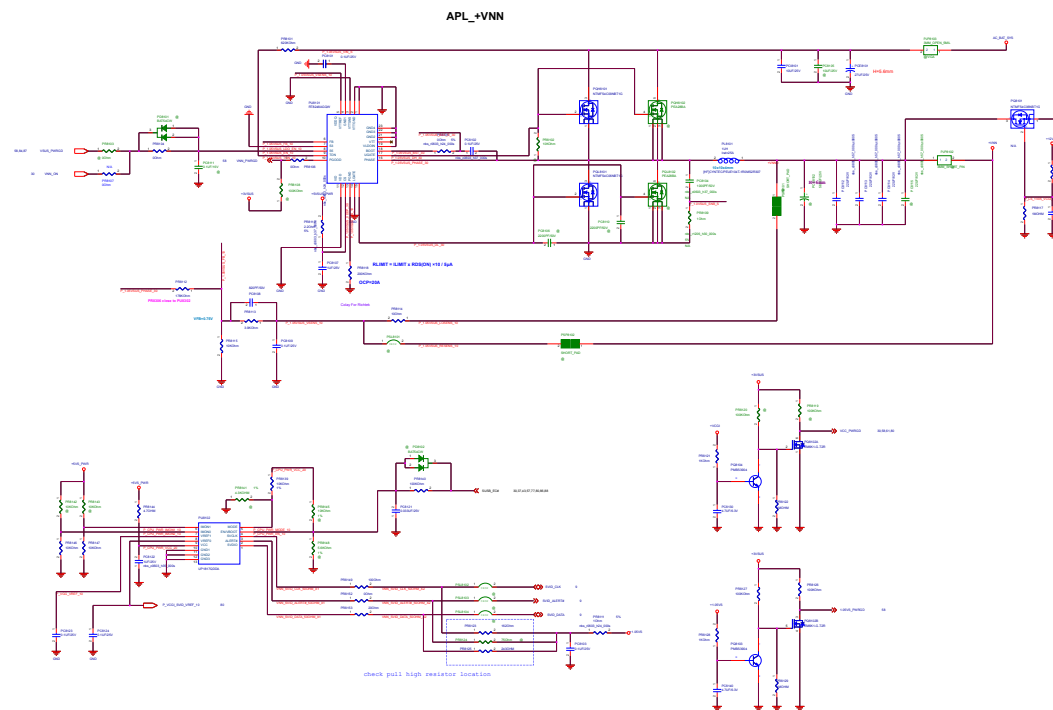
80_

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

74_VGA_nVIDIA_NVVDD_DISPLAY
75_VGA_nVIDIA_N16V/S_ROM,X
TAL
76_VGA_nVIDIA_N16V/S_GPIO
77_VGA_nVIDIA_N16V/S_POWE
R
78.
79_PROTECTION_2nd UP1905
80_PW_APL_VCGI_P
81_PW_APL_VCGI/VNN_P
82_PW_***
83_PW_
84_PW_+1.8VSUS/+1.24VSUS
85_PW_***
86_PW_+VDDQ/+VTT/+1.8V
87_PW_+3VSUS/+5VSUS
88_PW_LOAD SWITCH
89.PW_CHARGER(SN2867RUYR)
_P
90_PW_PROTECTION(w/o counte
r)
91_PW_+NVVDD (RT8820A)

Global Search

99_

93_

91_

90_

89.

88_

87_

86_

84_

81_

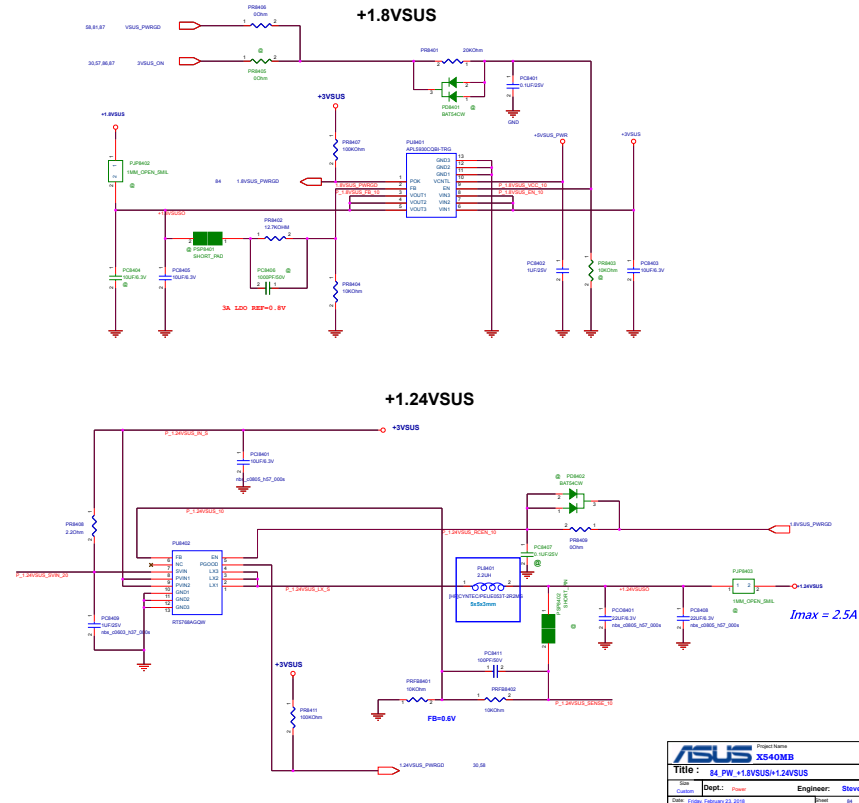
80_

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

74_VGA_nVIDIA_NVVDD_DISPLAY
75_VGA_nVIDIA_N16V/S_ROM,X
TAL
76_VGA_nVIDIA_N16V/S_GPIO
77_VGA_nVIDIA_N16V/S_POWE
R
78.
79_PROTECTION_2nd UP1905
80_PW_APL_VCGI_P
81_PW_APL_VCGI/VNN_P
82_PW_***
83_PW_
84_PW_+1.8VSUS/+1.24VSUS
85_PW_***
86_PW_+VDDQ/+VTT/+1.8V
87_PW_+3VSUS/+5VSUS
88_PW_LOAD SWITCH
89.PW_CHARGER(SN2867RUYR)
_P
90_PW_PROTECTION(w/o counte
r)
91_PW_+NVVDD (RT8820A)

Global Search

99_

93_

91_

90_

89.

88_

87_

86_

84_

81_

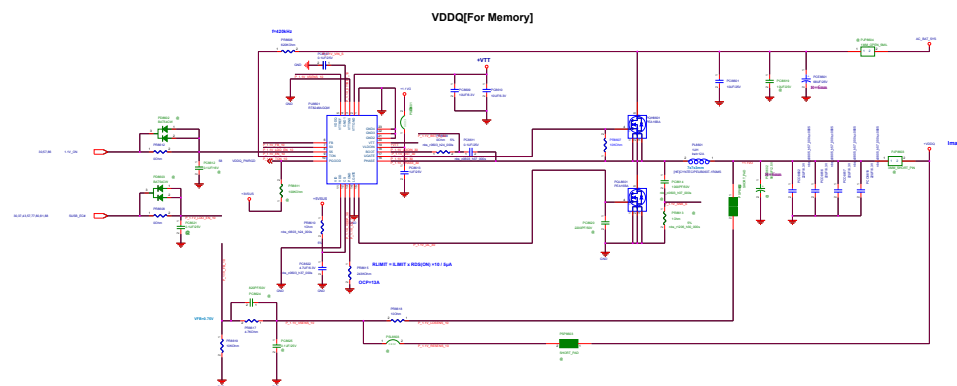
80_

Toggle FullScreen

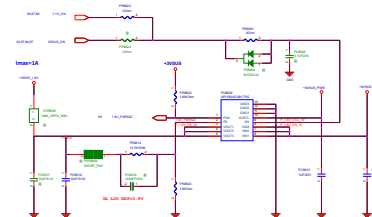
Pre Page

Next Page

MoveTo



+1.8V



ASUS	
Model	ASUS
Part No.	ASUS
Rev.	ASUS
Doc. No.	ASUS
Doc. Rev.	ASUS

Schematic Page List

Hide

74_VGA_nVIDIA_N16V/S_ROM,
Y
75_VGA_nVIDIA_N16V/S_ROM,X
TAL
76_VGA_nVIDIA_N16V/S_GPIO
77_VGA_nVIDIA_N16V/S_POWE
R
78.
79_PROTECTION_2nd UP1905
80_PW_APL_VCGI_P
81_PW_APL_VCGI/VNN_P
82_PW_***
83_PW_
84_PW_+1.8VSUS/+1.24VSUS
85_PW_***
86_PW_+VDDQ/+VTT/+1.8V
87_PW_+3VSUS/+5VSUS
88_PW_LOAD SWITCH
89.PW_CHARGER(SN2867RUYR)
_P
90_PW_PROTECTION(w/o counte
r)
91_PW_+NVVDD (RT8820A)

Global Search

99_

93_

91_

90_

89.

88_

87_

86_

84_

81_

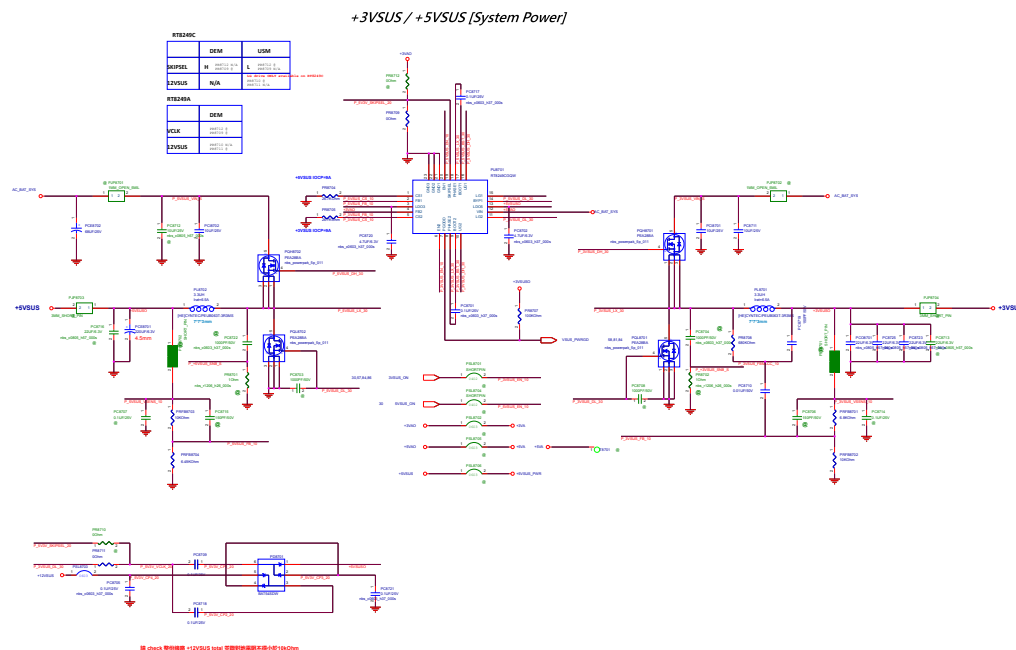
80_

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

Global Search

99_

93_

91_

90_

89.

88_

87_

86_

84_

81_

80_

Toggle FullScreen

Pre Page

Next Page

MoveTo

9

--	--

~~TF_VOR_NVIDIA_INOV70_DISPLAY~~
Y

75_VGA_nVIDIA_N16V/S_ROM,X
TAL

76_VGA_nVIDIA_N16V/S_GPIO

77_VGA_nVIDIA_N16V/S_POWE
R

78.

79_PROTECTION_2nd UP1905

80 PW APL VCGI P

81_PW_APL_VCGI/VNN_P

82_PW_***

83_PW_

84_PW_+1.8VSUS/+1.24VSUS

85_PW_***

86_PW_+VDDQ/+VTT/+1.8V

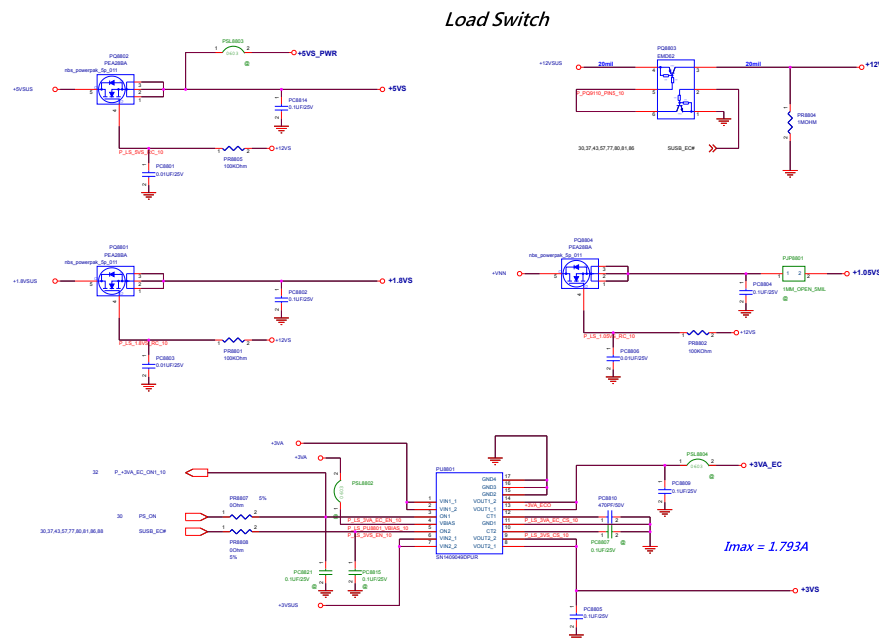
87 PW +3VSUS/+5VSUS

88_PW_LOAD SWITCH

89.PW_CHARGER(SN2867RUYR)
P

90_PW_PROTECTION(w/o counte
r)

91_PW_+NVVDD (RT8820A)


$$I_{max} = 1.793A$$

		Project Name		Sta	
		X540MB		5	
Title : 88_PW_LOAD SWITCH					
Size	Dept:	Power	Engineer:	Steve_Siao	
Custom					
Date:	Sales	Customer:	21	2018	
		Drawn	68	et	99

Schematic Page List

Hide

74_VGA_nVIDIA_N16V/S_POWER
75_VGA_nVIDIA_N16V/S_ROM,XTAL
76_VGA_nVIDIA_N16V/S_GPIO
77_VGA_nVIDIA_N16V/S_POWER
78.
79_PROTECTION_2nd UP1905
80_PW_APL_VCGI_P
81_PW_APL_VCGI/VNN_P
82_PW_***
83_PW_
84_PW_+1.8VSUS/+1.24VSUS
85_PW_***
86_PW_+VDDQ/+VTT/+1.8V
87_PW_+3VSUS/+5VSUS
88_PW_LOAD SWITCH
89.PW_CHARGER(SN2867RUYR)_P
90_PW_PROTECTION(w/o counter)
91_PW_+NVVDD (RT8820A)

Global Search

99_

93_

91_

90_

89.

88_

87_

86_

84_

81_

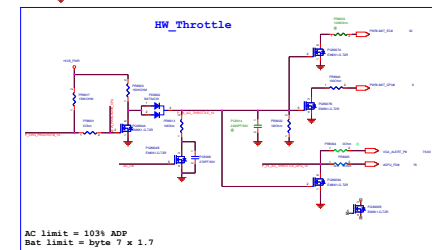
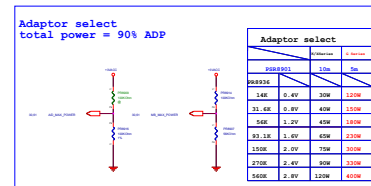
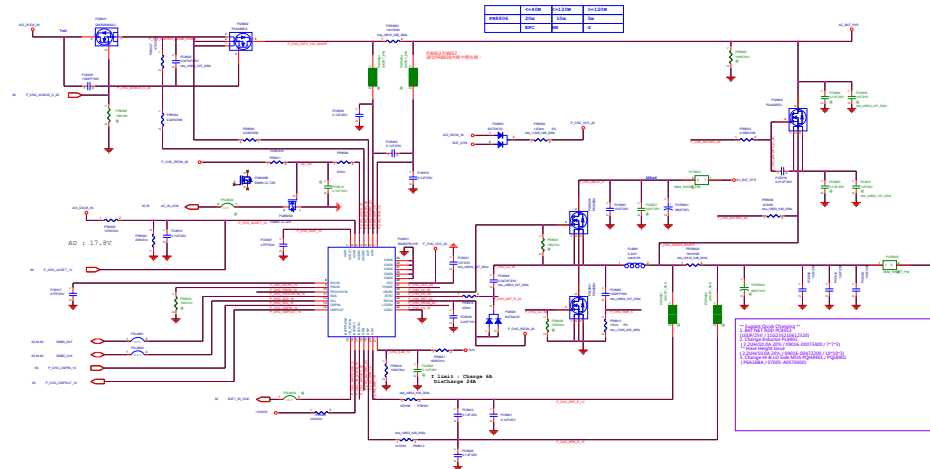
80_

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

74_VGA_nVIDIA_NVVO_DISPLAY
75_VGA_nVIDIA_N16V/S_ROM,X
TAL
76_VGA_nVIDIA_N16V/S_GPIO
77_VGA_nVIDIA_N16V/S_POWE
R
78.
79_PROTECTION_2nd UP1905
80_PW_APL_VCGI_P
81_PW_APL_VCGI/VNN_P
82_PW_***
83_PW_
84_PW_+1.8VSUS/+1.24VSUS
85_PW_***
86_PW_+VDDQ/+VTT/+1.8V
87_PW_+3VSUS/+5VSUS
88_PW_LOAD SWITCH
89.PW_CHARGER(SN2867RUYR)
_P
90_PW_PROTECTION(w/o counte
r)
91_PW_+NVVDD (RT8820A)

Global Search

99_

93_

91_

90_

89.

88_

87_

86_

84_

81_

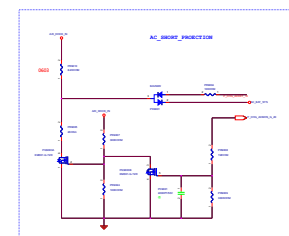
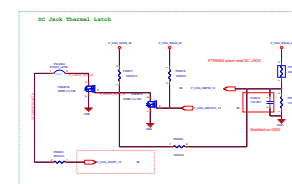
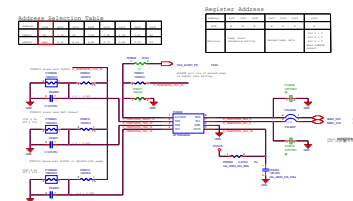
80_

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

~~RT_FOR_NVIDIA_INTO_VIO_DISPLAY~~
Y

75_VGA_nVIDIA_N16V/S_ROM,X
TAL

76_VGA_nVIDIA_N16V/S_GPIO

77_VGA_nVIDIA_N16V/S_POWE
R

78.

79_PROTECTION_2nd UP1905

80 PW APL VCGI P

81_PW_APL_VCGI/MNN_P

82_PW_***

83_PW_

84_PW_+1.8VSUS/+1.24VSUS

85_PW_***

86_PW_+VDDQ/+VTT/+1.8V

87 PW +3VSUS/+5VSUS

88 PW LOAD SWITCH

89.PW_CHARGER(SN2867RUYR)
P

90_PW_PROTECTION(w/o counte
r)

91_PW_+NVVDD (RT8820A)

Global Search

99

93

91

90

89.

88

87

86

84

81

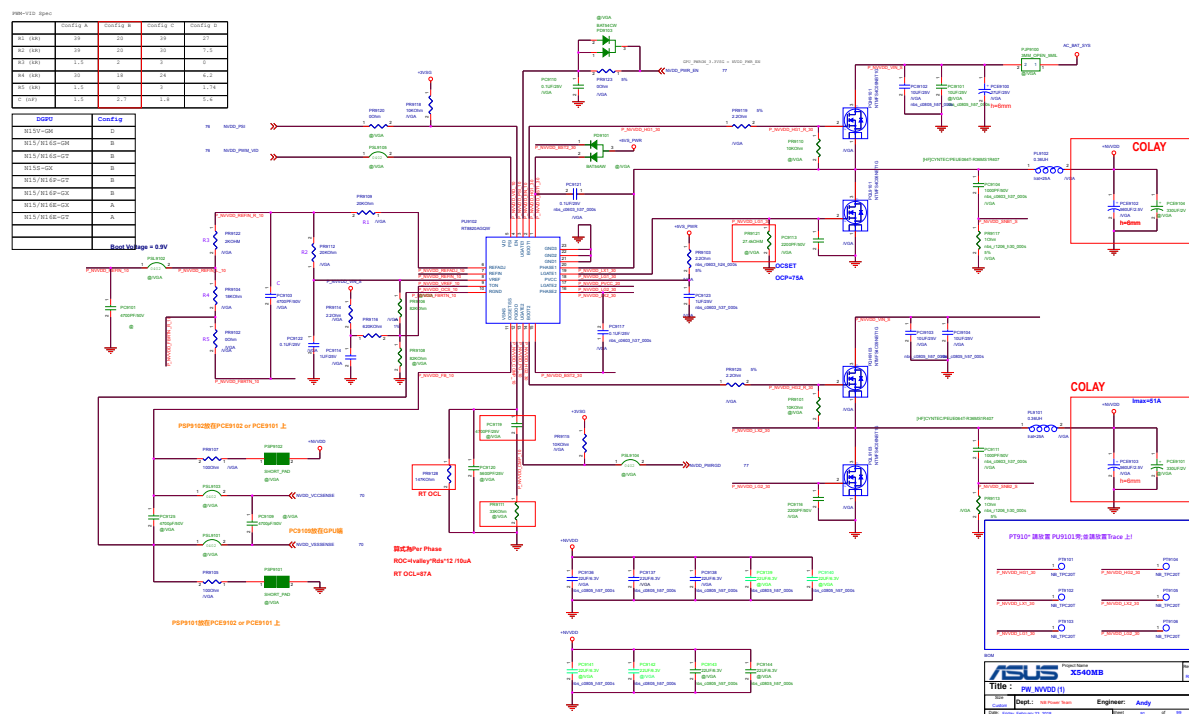
80

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

74_VGA_nVIDIA_NVVDD_DISPLAY
75_VGA_nVIDIA_N16V/S_ROM,X
TAL
76_VGA_nVIDIA_N16V/S_GPIO
77_VGA_nVIDIA_N16V/S_POWE
R
78.
79_PROTECTION_2nd UP1905
80_PW_APL_VCGI_P
81_PW_APL_VCGI/VNN_P
82_PW_***
83_PW_
84_PW_+1.8VSUS/+1.24VSUS
85_PW_***
86_PW_+VDDQ/+VTT/+1.8V
87_PW_+3VSUS/+5VSUS
88_PW_LOAD SWITCH
89.PW_CHARGER(SN2867RUYR)
_P
90_PW_PROTECTION(w/o counte
r)
91_PW_+NVVDD (RT8820A)

Global Search

99_

93_

91_

90_

89.

88_

87_

86_

84_

81_

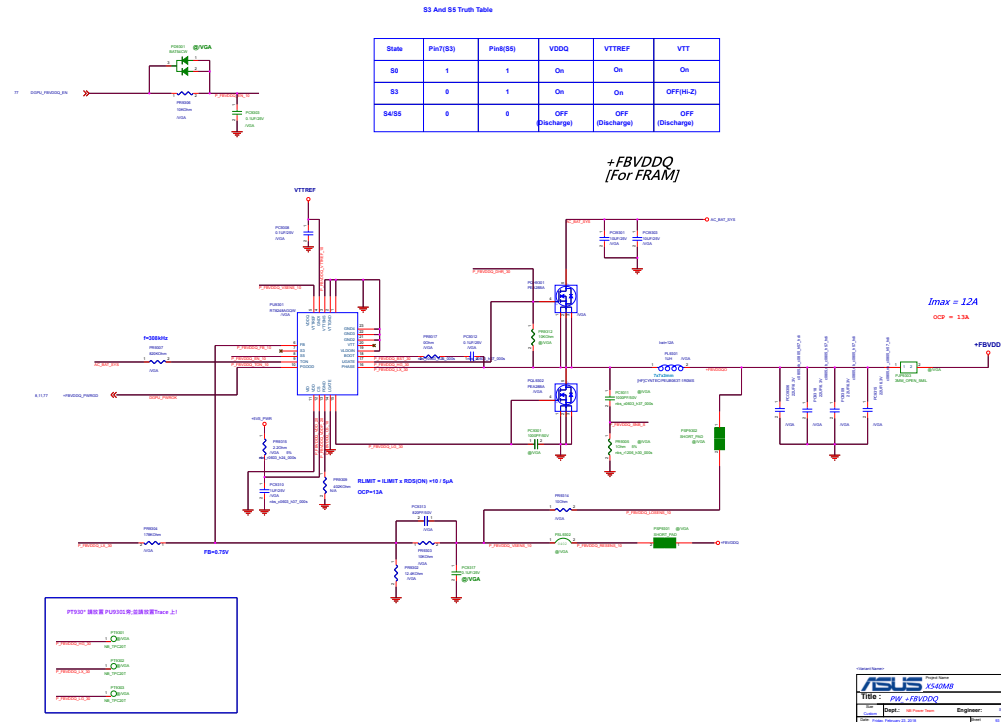
80_

Toggle FullScreen

Pre Page

Next Page

MoveTo



Schematic Page List

Hide

~~TF_VOR_IVIDIA_INOVVO_DISPLAY~~
Y

75_VGA_nVIDIA_N16V/S_ROM,X
TAL

76_VGA_nVIDIA_N16V/S_GPIO

77_VGA_nVIDIA_N16V/S_POWE
R

78.

79_PROTECTION_2nd UP1905

80_PW_APL_VCGI_P

81_PW_APL_VCGI/MNN_P

82_PW_***

83_PW_

84_PW_+1.8VSUS/+1.24VSUS

85_PW_***

86_PW_+VDDQ/+VTT/+1.8V

87 PW +3VSUS/+5VSUS

88 PW LOAD SWITCH

89.PW_CHARGER(SN2867RUYR)
P

90_PW_PROTECTION(w/o counte
r)

91_PW_+NVVDD (RT8820A)

Global Search

99_

93_

91_

90_

89.

88_

87_

86

84_

81_

80_

Toggle FullScreen

Pre Page

Next Page

MoveTo

